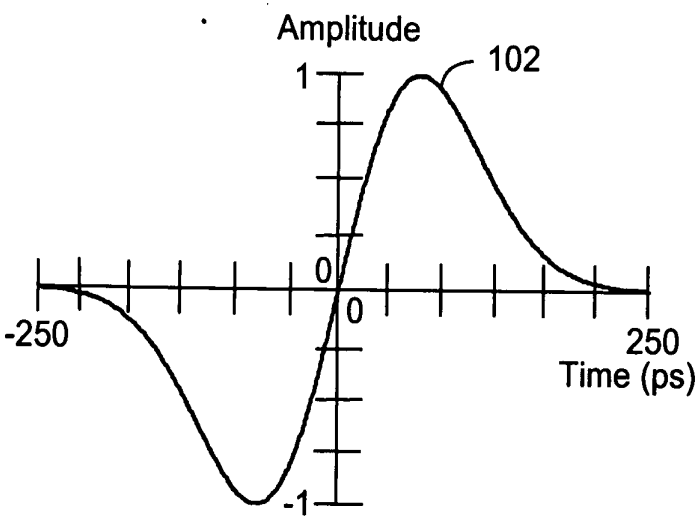

Amplitude
1
102
0
0
-250
250
Time (ps)
-1

FIG. 1A

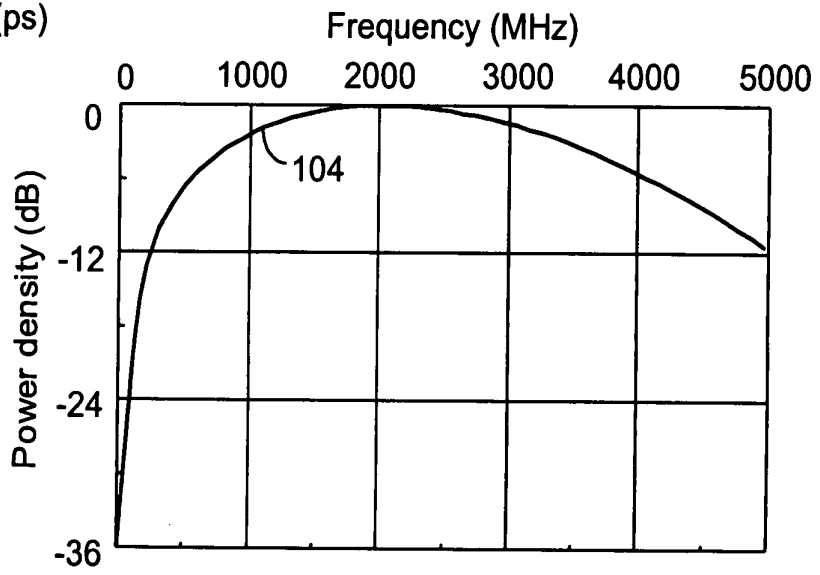

Frequency (MHz)
0
1000
2000
3000
4000
5000
0
-12
-24
-36
Power density (dB)
104

FIG. 1B

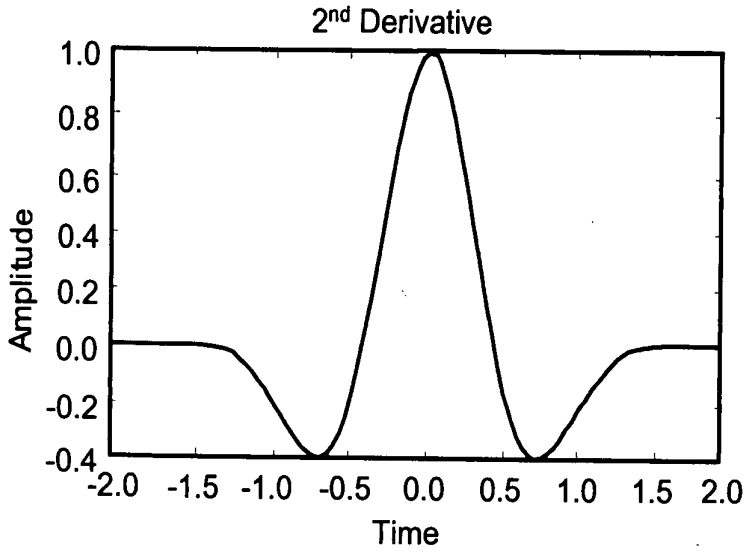

2nd Derivative
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
Amplitude
-2.0 -1.5 -1.0 -0.5 0.0 0.5 1.0 1.5 2.0
Time

FIG. 1C

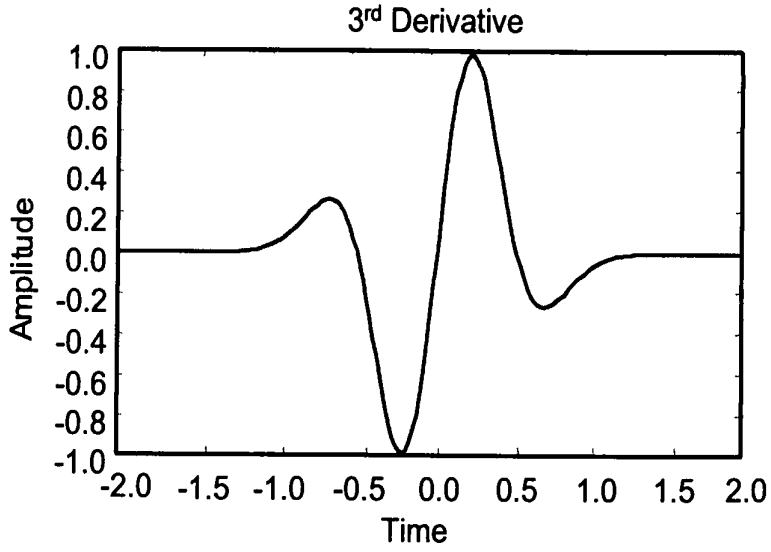

3rd Derivative
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
Amplitude
-2.0 -1.5 -1.0 -0.5 0.0 0.5 1.0 1.5 2.0
Time

FIG. 1D

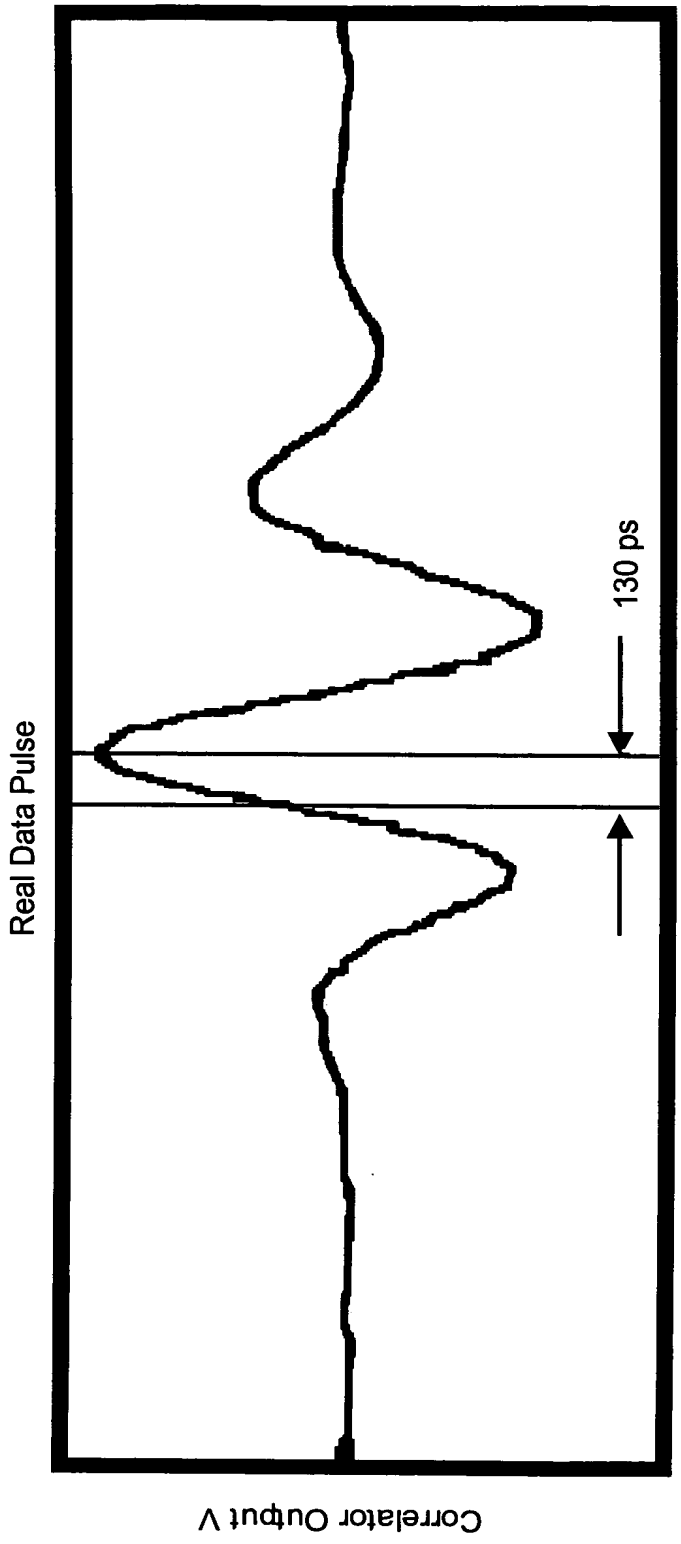


FIG. 1E

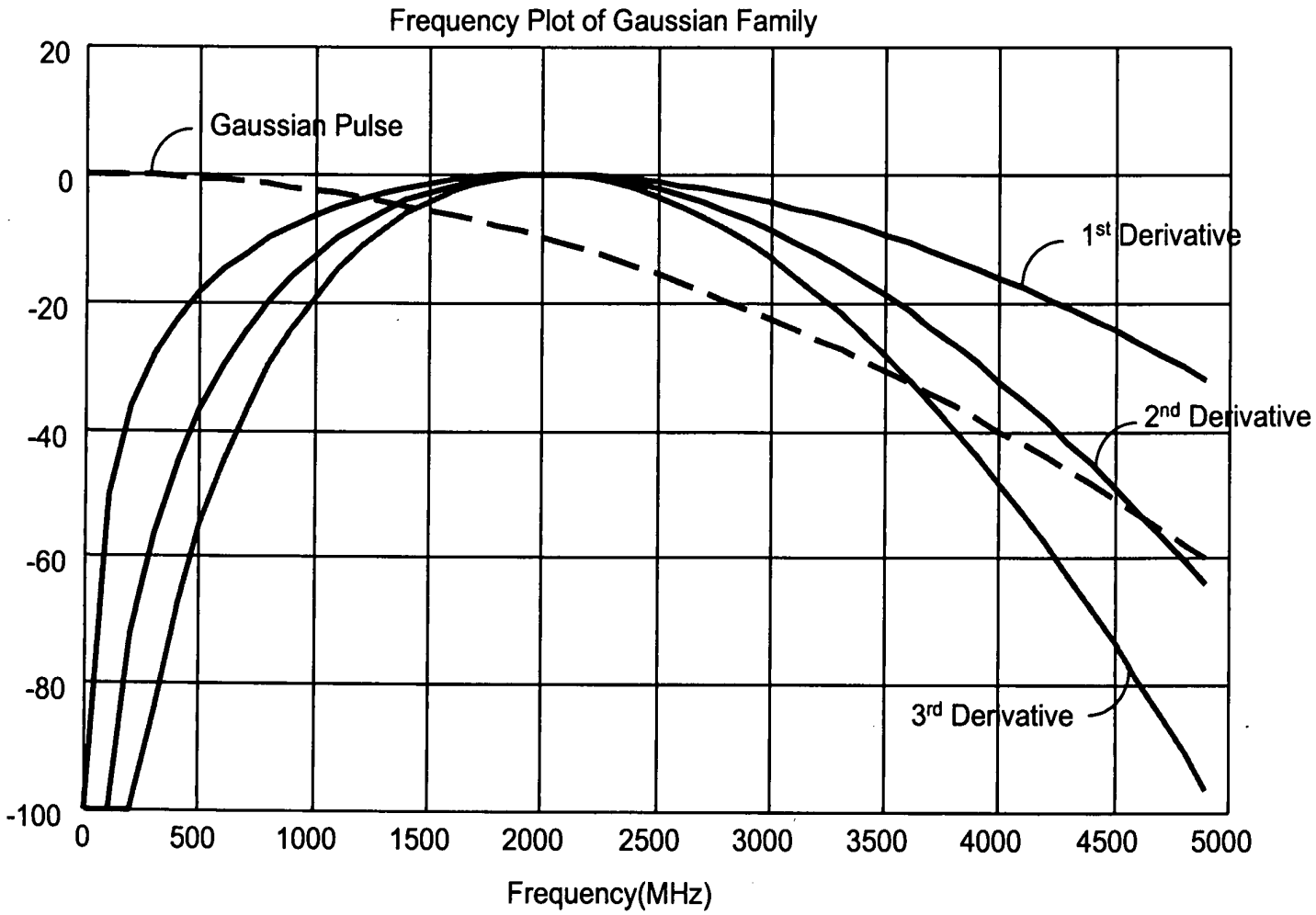

Frequency Plot of Gaussian Family
20
0
-20
-40
-60
-80
-100
0
500
1000
1500
2000
2500
3000
3500
4000
4500
5000
Frequency(MHz)
Gaussian Pulse
1st Derivative
2nd Derivative
3rd Derivative

FIG. 1F

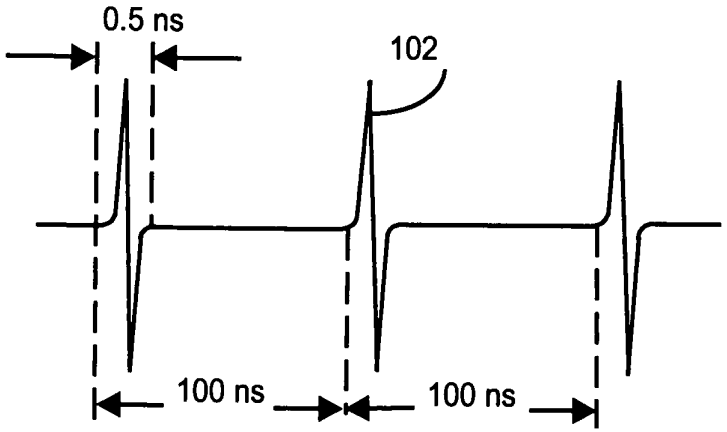


FIG. 2A

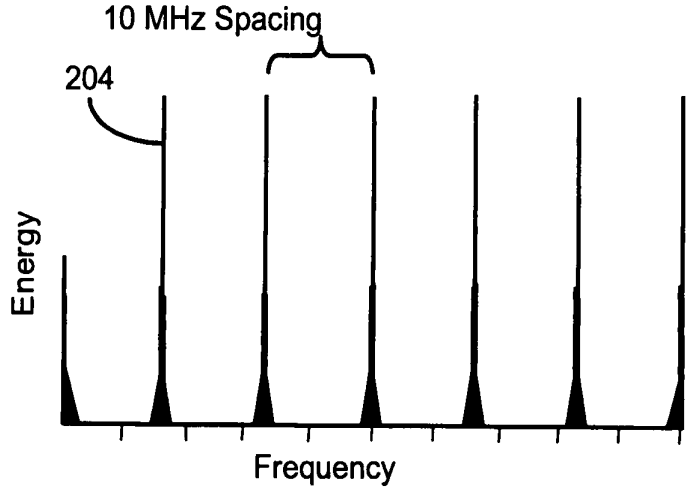


FIG. 2B

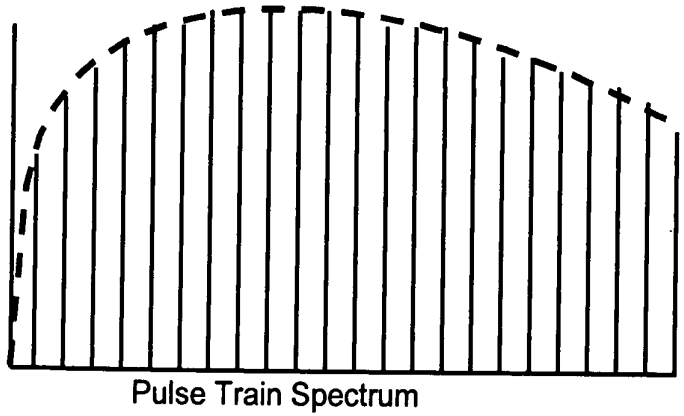


FIG. 2C

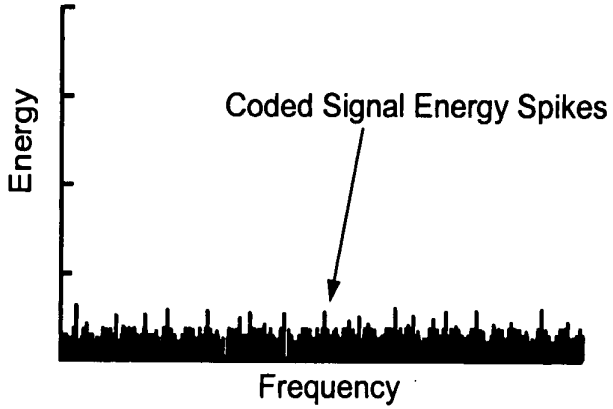


FIG. 2D

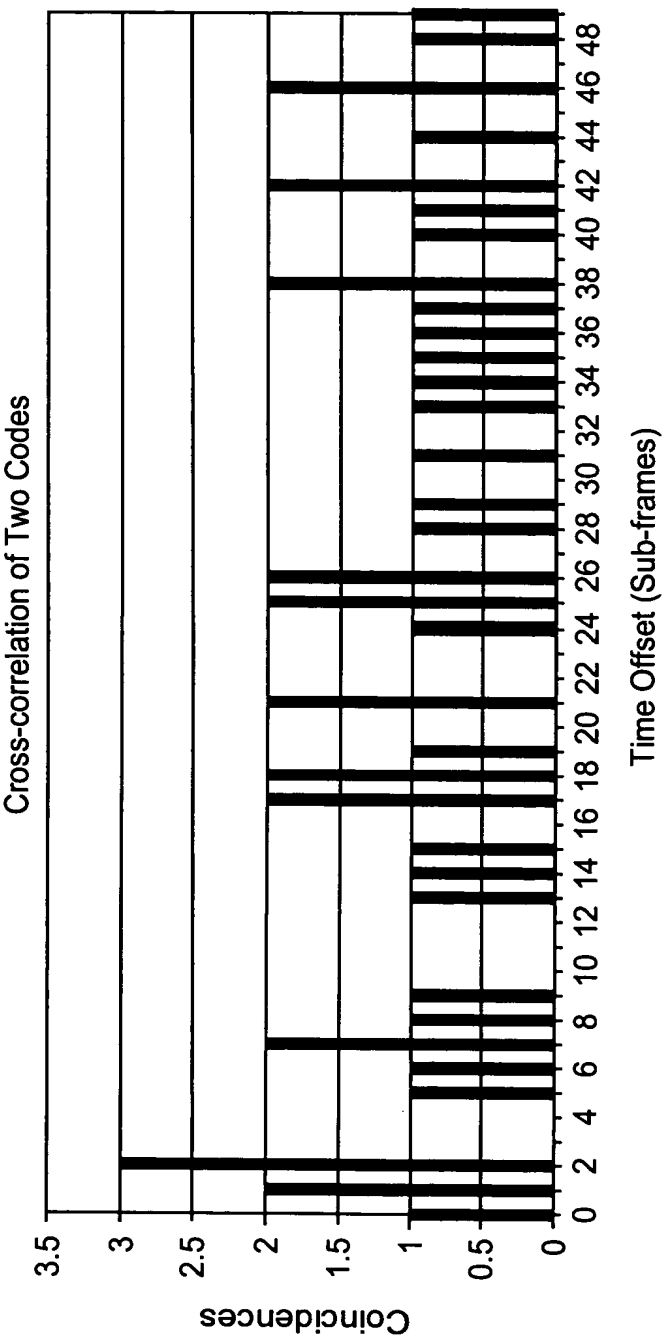
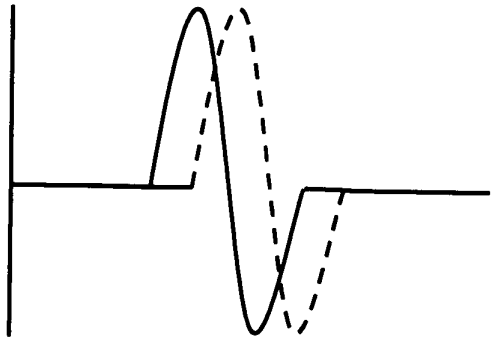
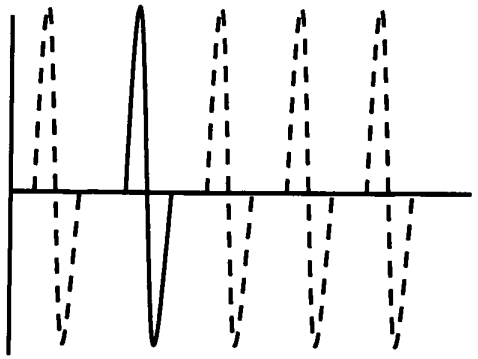

Cross-correlation of Two Codes
Coincidences
Time Offset (Sub-frames)
3.5
3
2.5
2
1.5
1
0.5
0
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48

FIG. 3



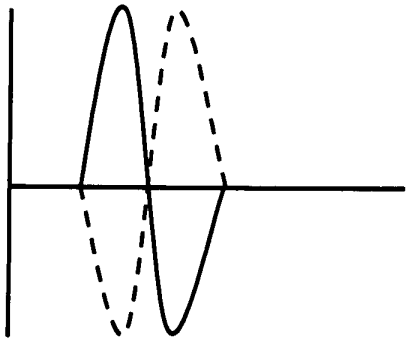
Early – Late Modulation

FIG. 4A



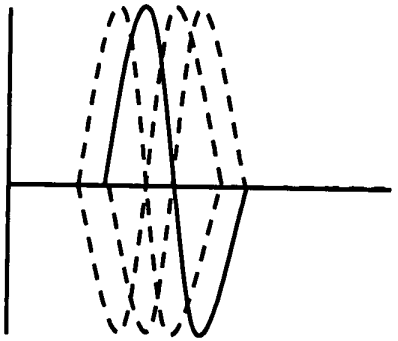
One of Many Modulation

FIG. 4B



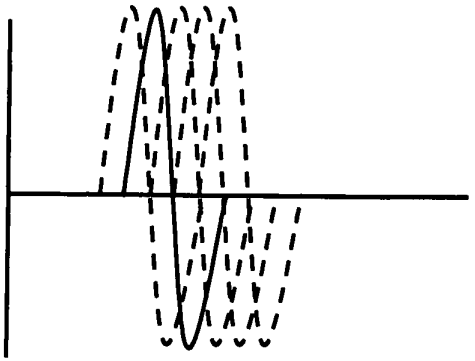
Flip Modulation

FIG. 4C



Quad Flip Modulation

FIG. 4D



Vector Modulation

FIG. 4E

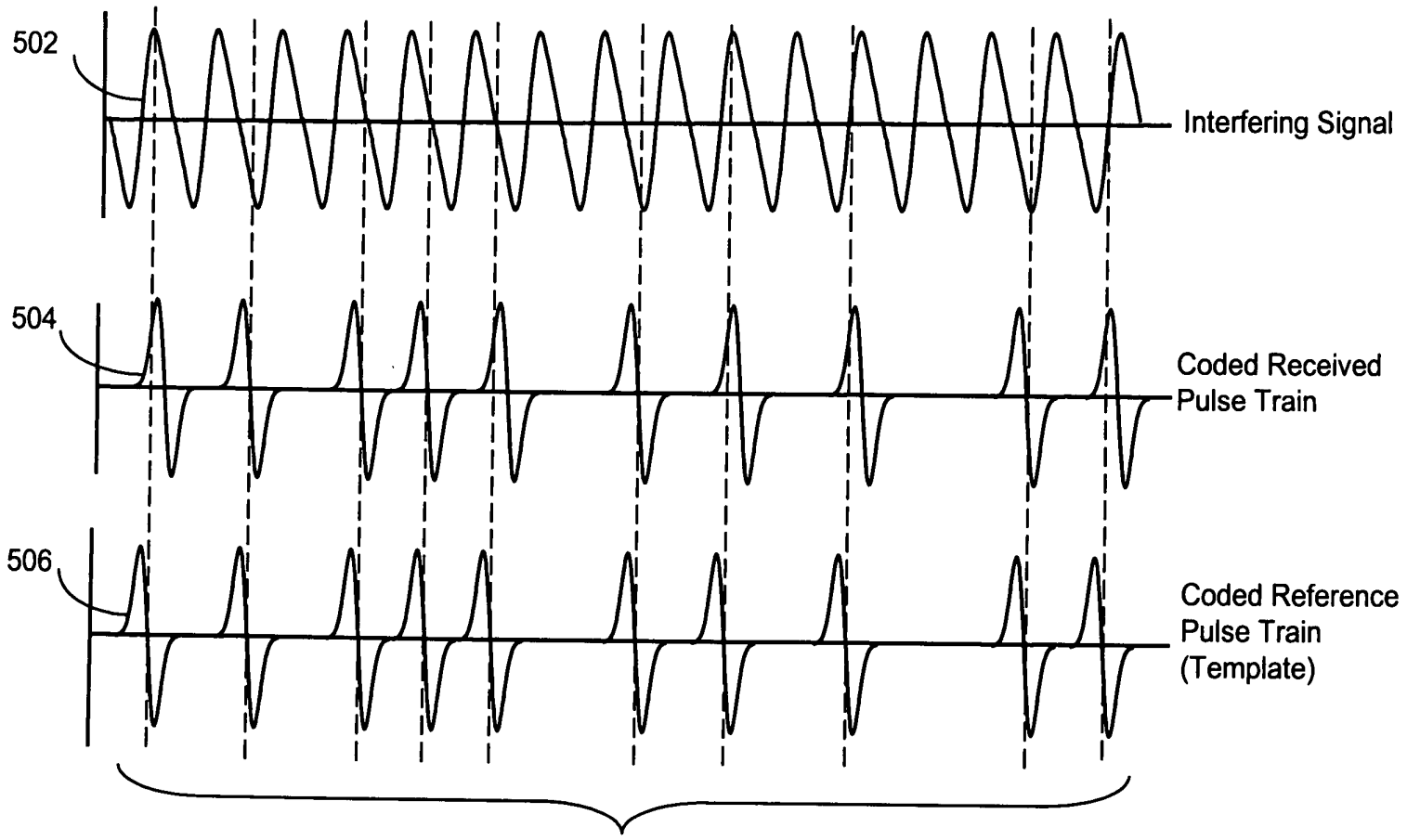

502
Interfering Signal
504
Coded Received
Pulse Train
506
Coded Reference
Pulse Train
(Template)

FIG. 5A

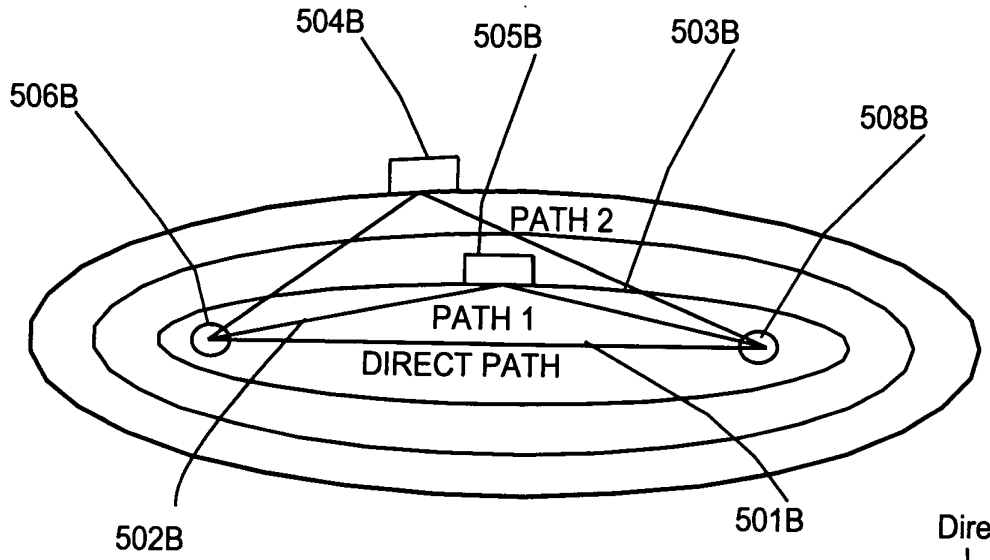

504B
505B
503B
506B
508B
PATH 2
PATH 1
DIRECT PATH
502B
501B

FIG. 5B

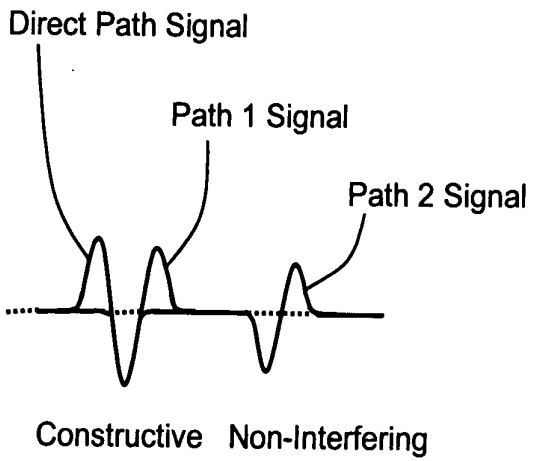

Direct Path Signal
Path 1 Signal
Path 2 Signal
Constructive
Non-Interfering

FIG. 5C

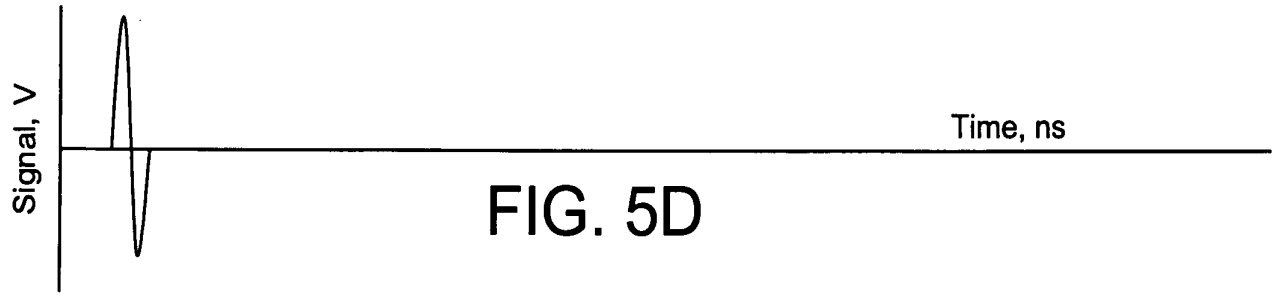


FIG. 5D

FIG. 5E

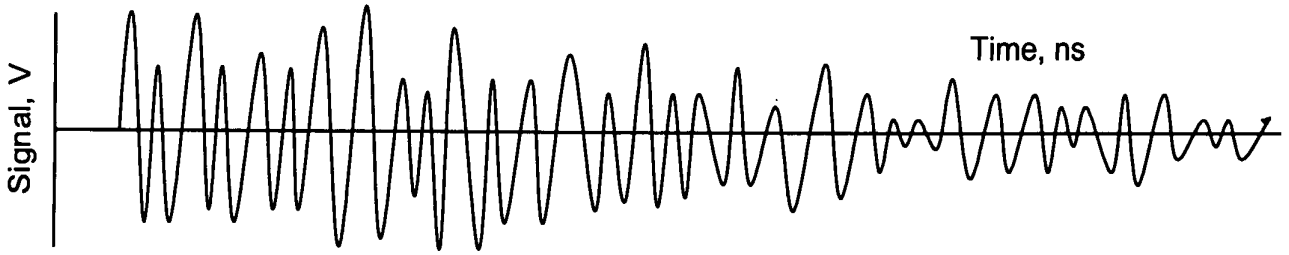


FIG. 5F

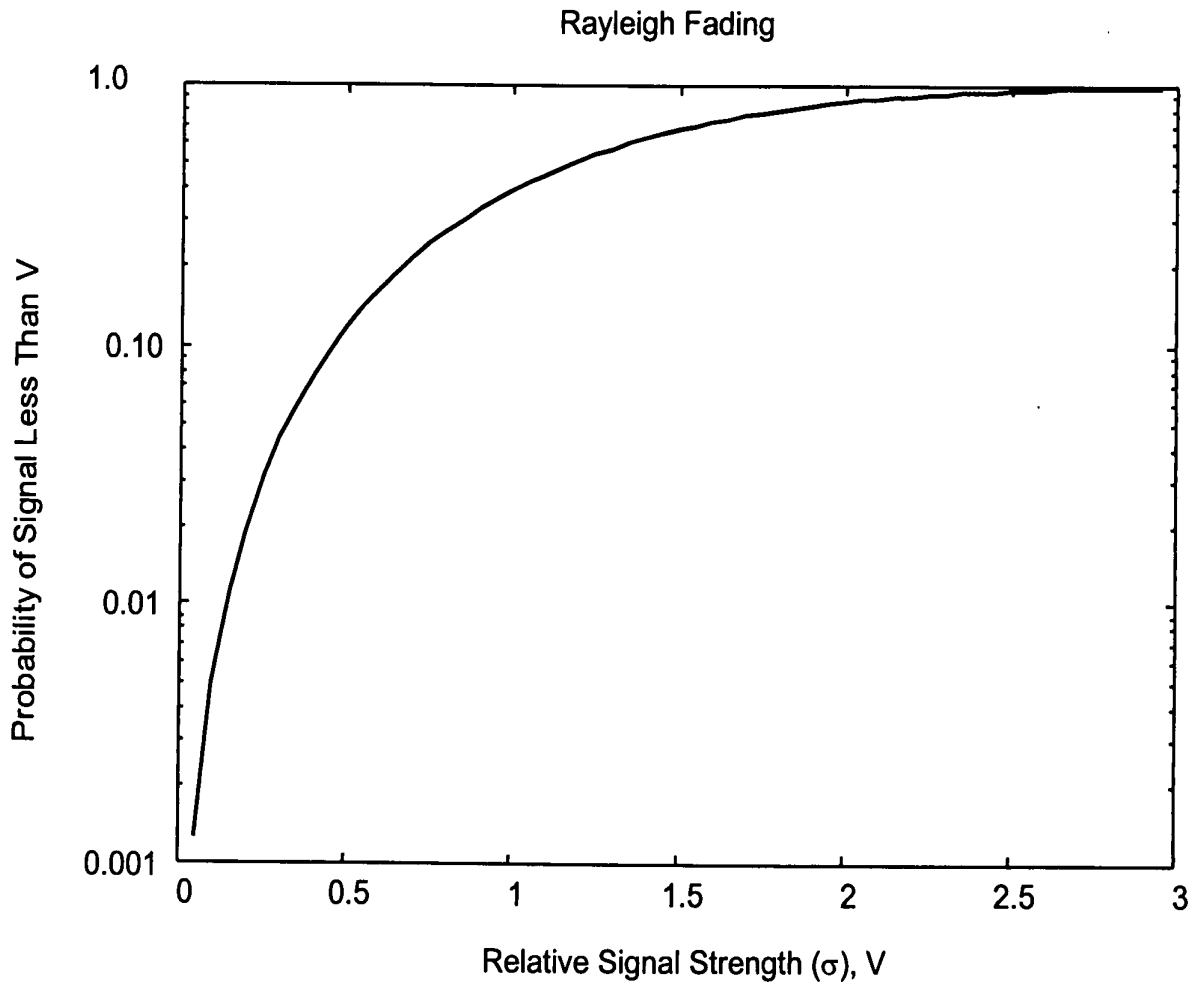

Rayleigh Fading
1.0
0.10
0.01
0.001
Probability of Signal Less Than V
0
0.5
1
1.5
2
2.5
3
Relative Signal Strength (σ), V

Fig. 5G

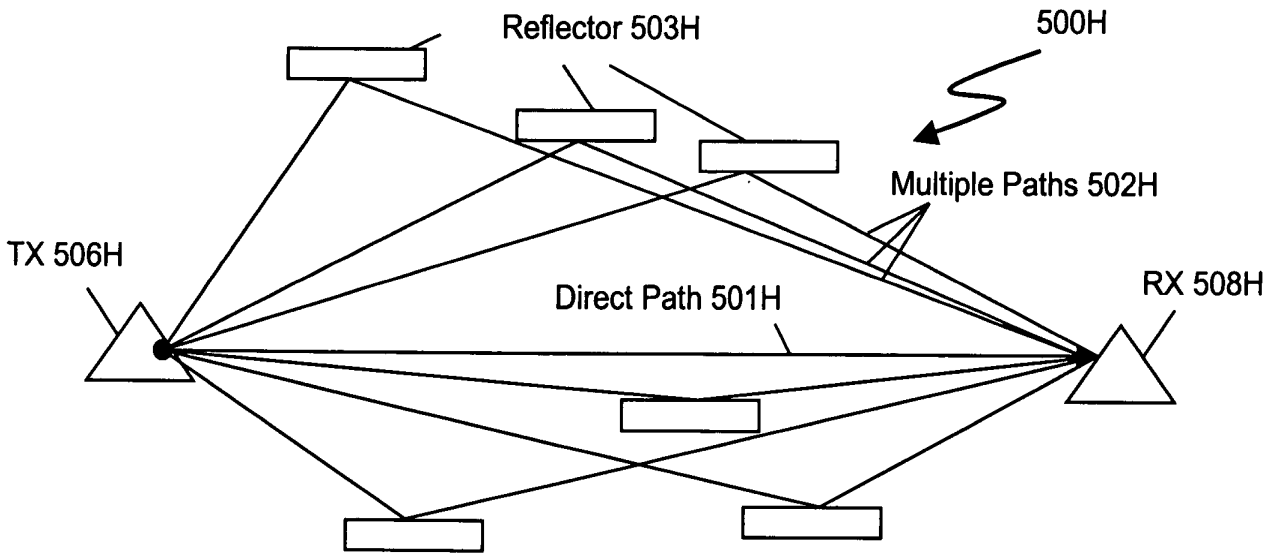

Reflector 503H
500H
Multiple Paths 502H
TX 506H
Direct Path 501H
RX 508H

FIG. 5H

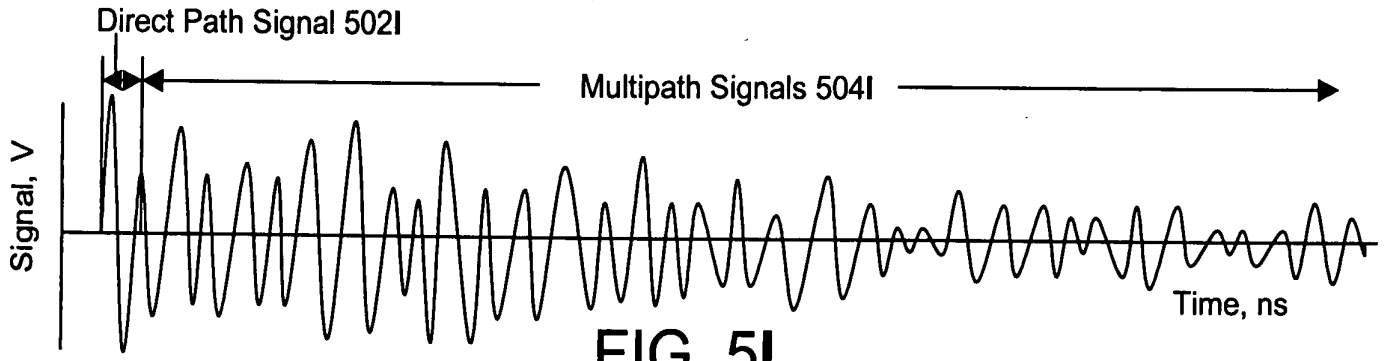

Direct Path Signal 502I
Multipath Signals 504I
Signal, V
Time, ns

FIG. 5I

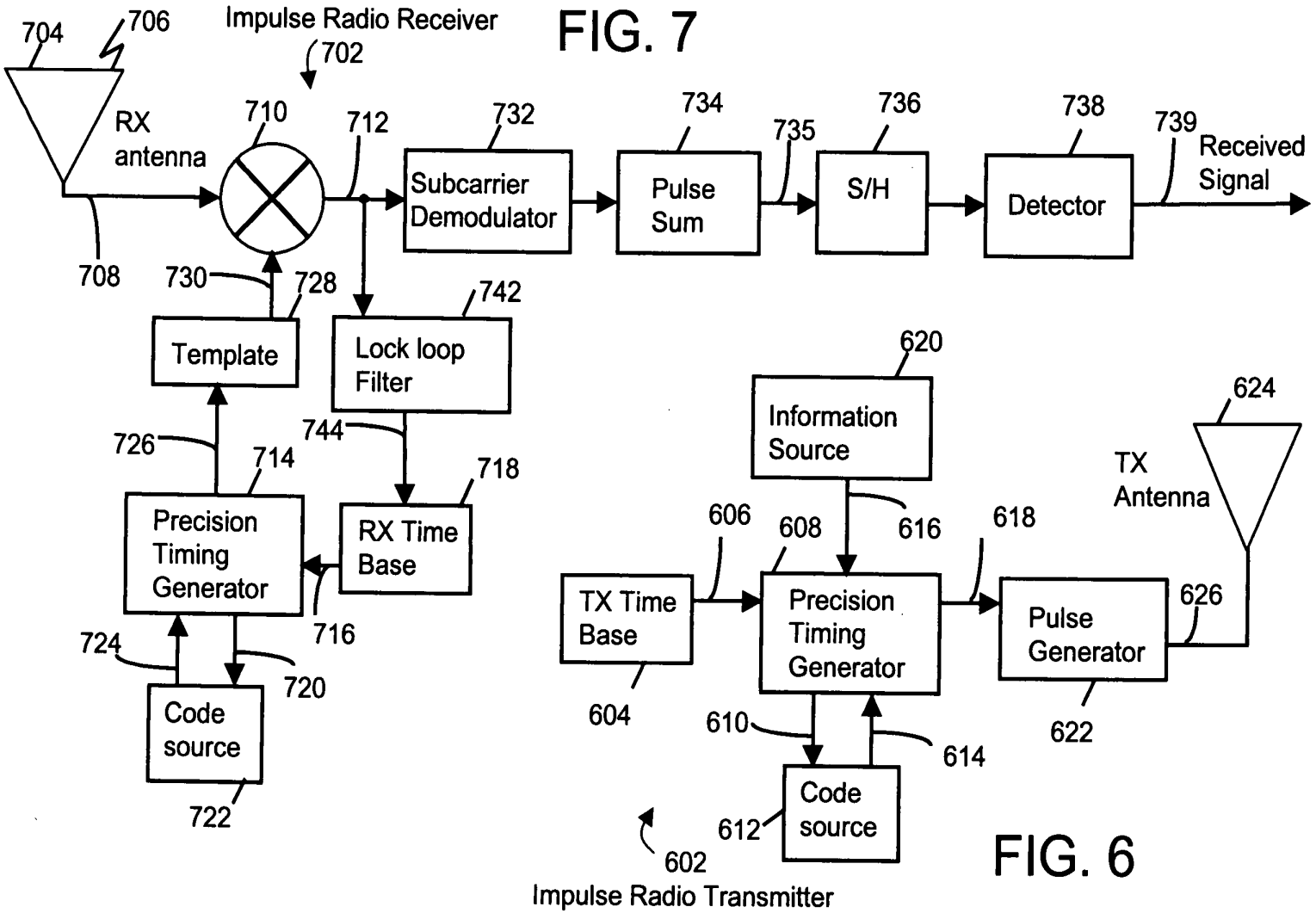

Impulse Radio Receiver
702
704
706
RX antenna
708
710
712
732
Subcarrier Demodulator
734
Pulse Sum
735
736
S/H
738
Detector
739
Received Signal
730
728
742
Template
Lock loop Filter
726
744
714
718
Precision Timing Generator
RX Time Base
716
724
720
Code source
722
620
Information Source
624
TX Antenna
606
608
616
618
TX Time Base
Precision Timing Generator
Pulse Generator
626
604
610
614
622
Code source
612
602
Impulse Radio Transmitter

FIG. 7

FIG. 6

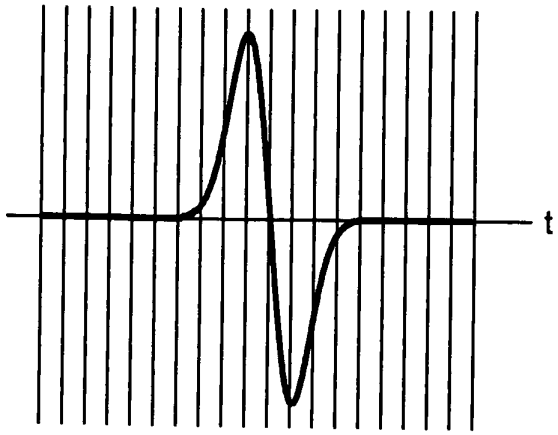


FIG. 8A

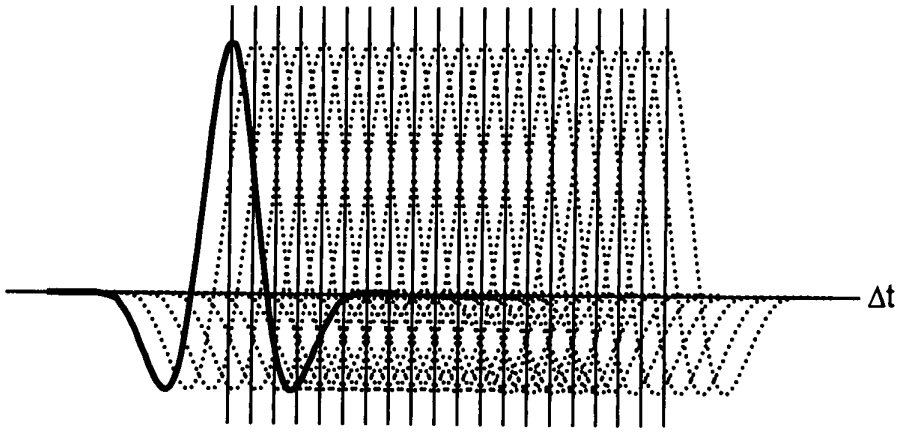


FIG. 8B

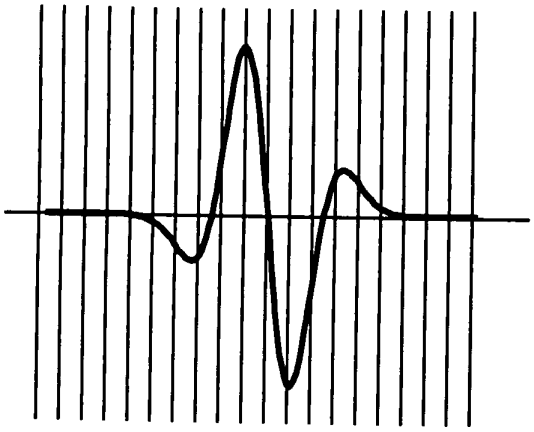


FIG. 8C

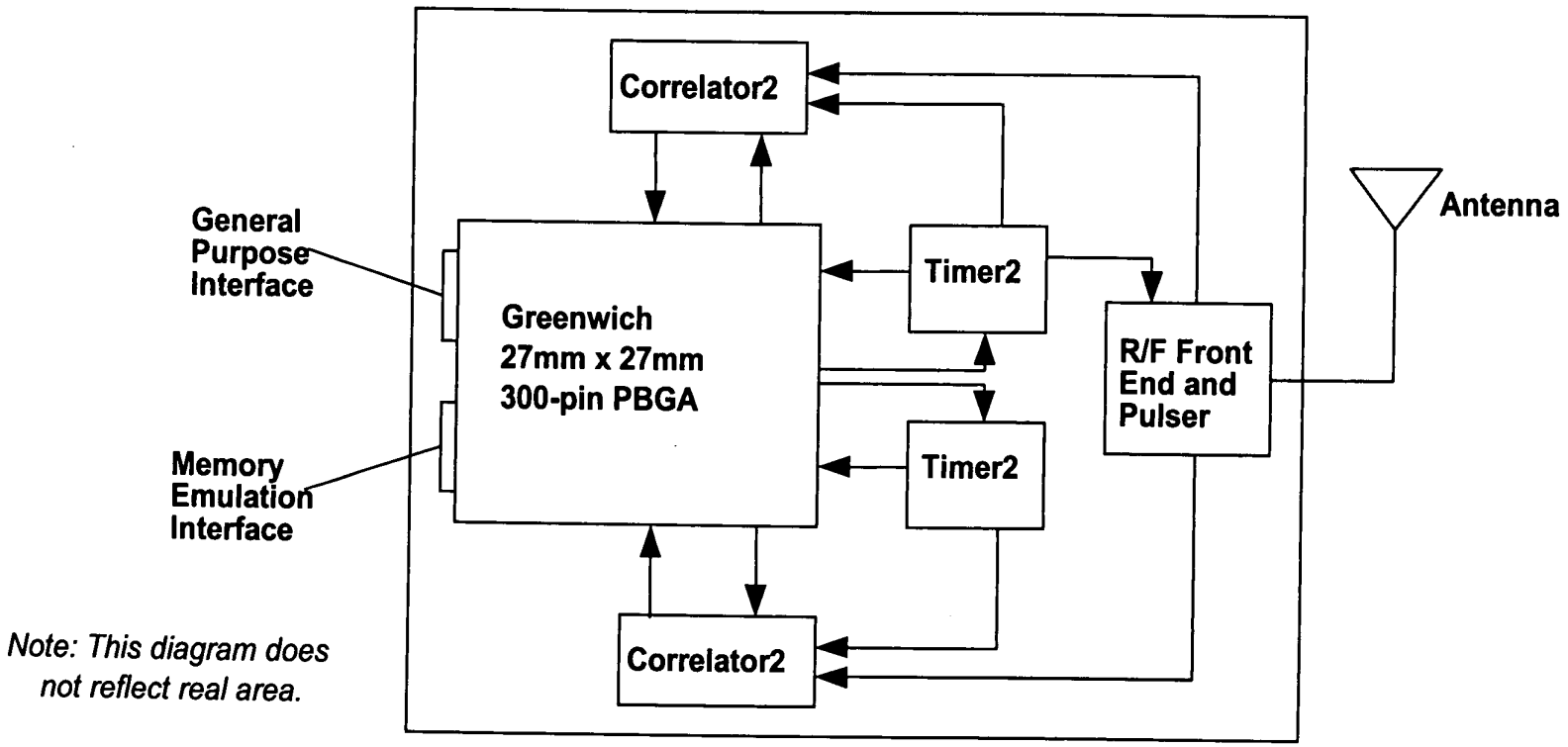
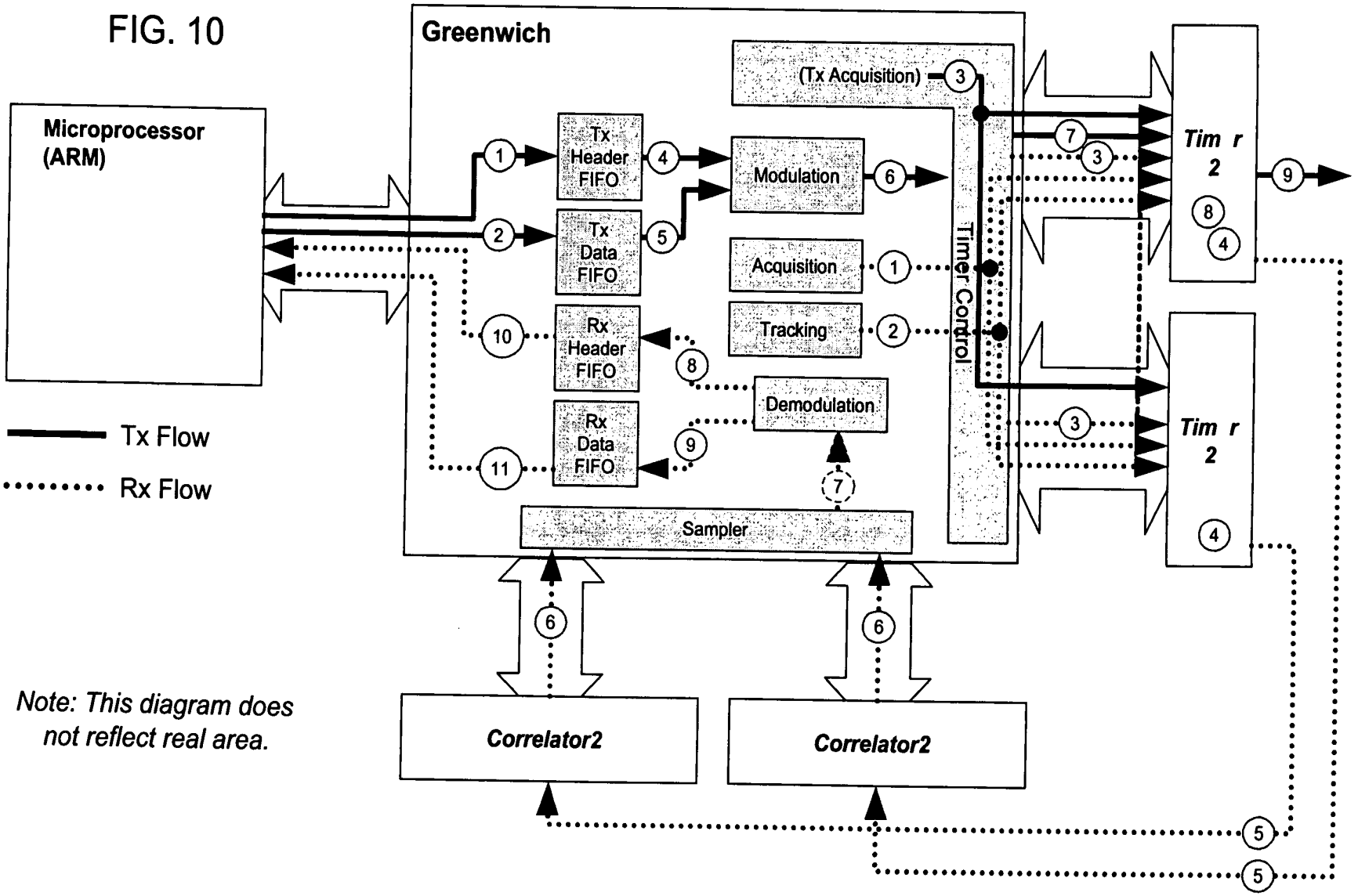

Correlator2
General Purpose Interface
Greenwich 27mm x 27mm 300-pin PBGA
Timer2
Timer2
R/F Front End and Pulser
Antenna
Memory Emulation Interface
Correlator2
Note: This diagram does not reflect real area.

FIG. 9

FIG. 10


Greenwich
Microprocessor (ARM)
Tx Header FIFO
Tx Data FIFO
Rx Header FIFO
Rx Data FIFO
Modulation
Acquisition
Tracking
Demodulation
(Tx Acquisition)
Timer Control
Sampler
Tim r 2
Tim r 2
Correlator2
Correlator2
Tx Flow
Rx Flow
Note: This diagram does not reflect real area.

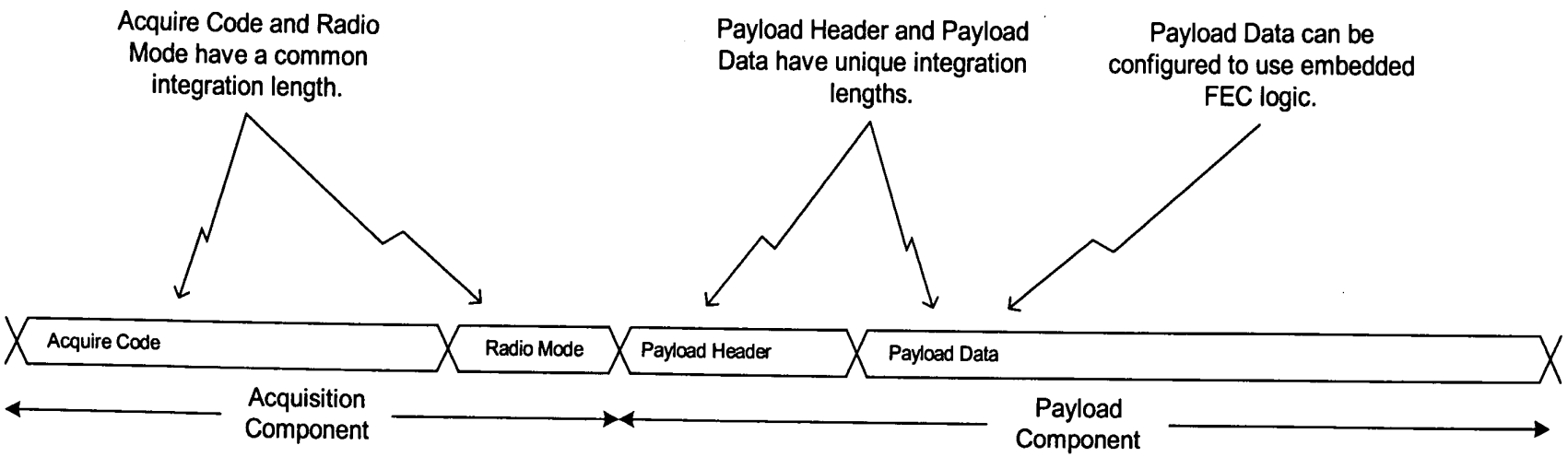

Acquire Code and Radio Mode have a common integration length.
Payload Header and Payload Data have unique integration lengths.
Payload Data can be configured to use embedded FEC logic.
Acquire Code
Radio Mode
Payload Header
Payload Data
Acquisition Component
Payload Component

FIG. 11

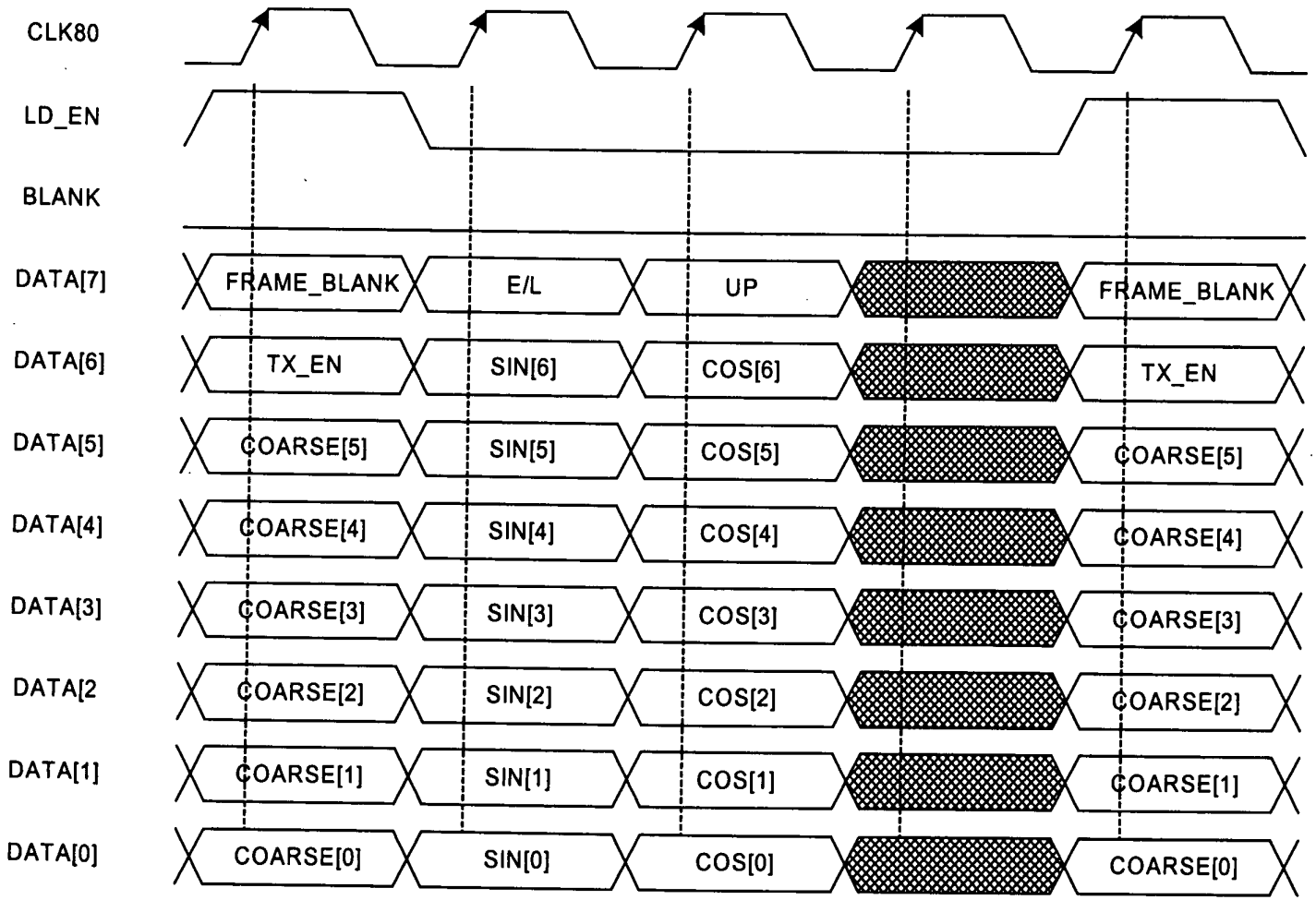

CLK80
LD_EN
BLANK
DATA[7]
DATA[6]
DATA[5]
DATA[4]
DATA[3]
DATA[2
DATA[1]
DATA[0]
FRAME_BLANK
E/L
UP
FRAME_BLANK
TX_EN
SIN[6]
COS[6]
TX_EN
COARSE[5]
SIN[5]
COS[5]
COARSE[5]
COARSE[4]
SIN[4]
COS[4]
COARSE[4]
COARSE[3]
SIN[3]
COS[3]
COARSE[3]
COARSE[2]
SIN[2]
COS[2]
COARSE[2]
COARSE[1]
SIN[1]
COS[1]
COARSE[1]
COARSE[0]
SIN[0]
COS[0]
COARSE[0]

FIG. 12

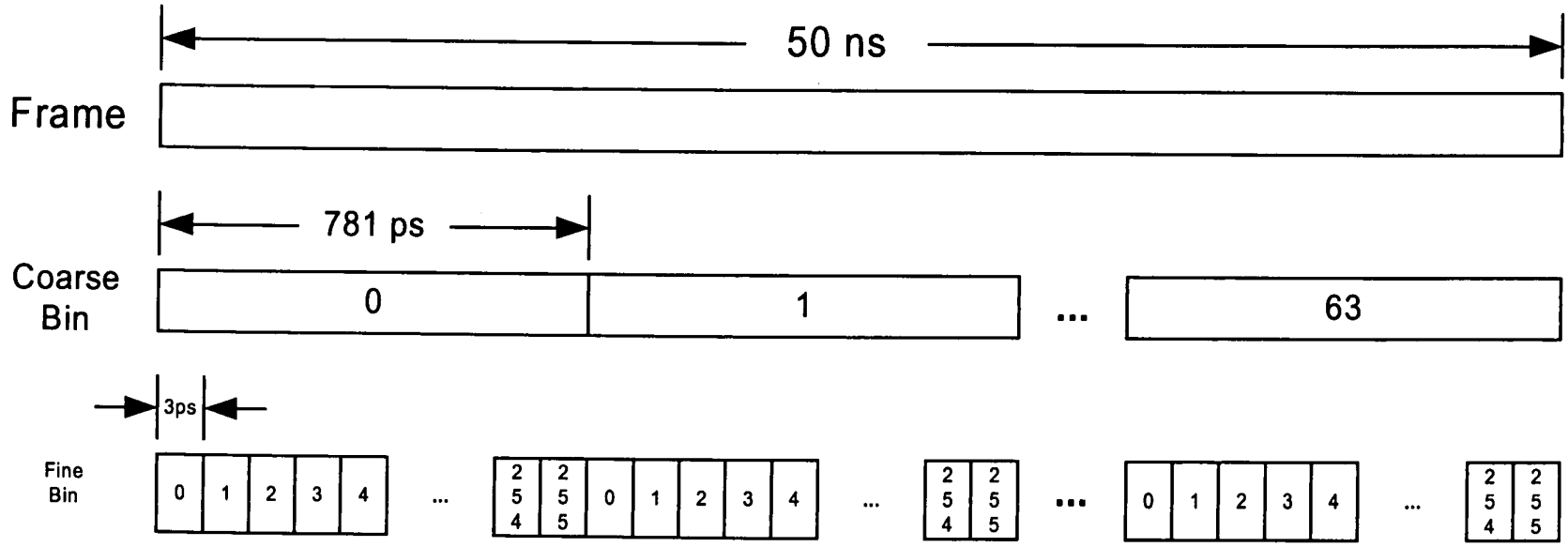

50 ns
Frame
781 ps
Coarse Bin
0
1
...
63
3ps
Fine Bin
0 1 2 3 4 ... 254 255 0 1 2 3 4 ... 254 255 ... 0 1 2 3 4 ... 254 255

FIG. 13

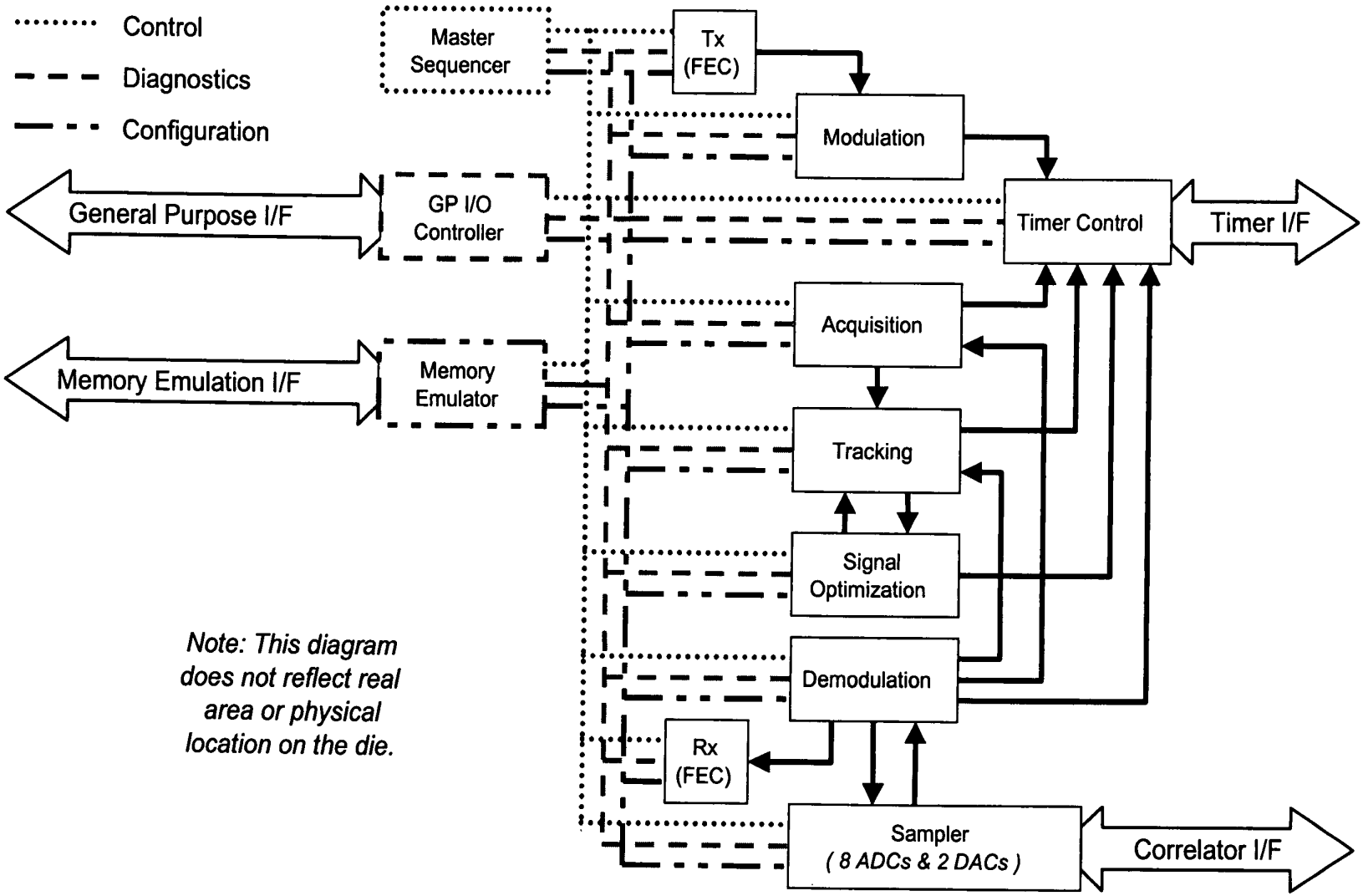

Control
Diagnostics
Configuration
Master Sequencer
Tx (FEC)
Modulation
General Purpose I/F
GP I/O Controller
Timer Control
Timer I/F
Acquisition
Memory Emulation I/F
Memory Emulator
Tracking
Signal Optimization
Demodulation
Rx (FEC)
Sampler (8 ADCs & 2 DACs)
Correlator I/F
Note: This diagram does not reflect real area or physical location on the die.

FIG. 14

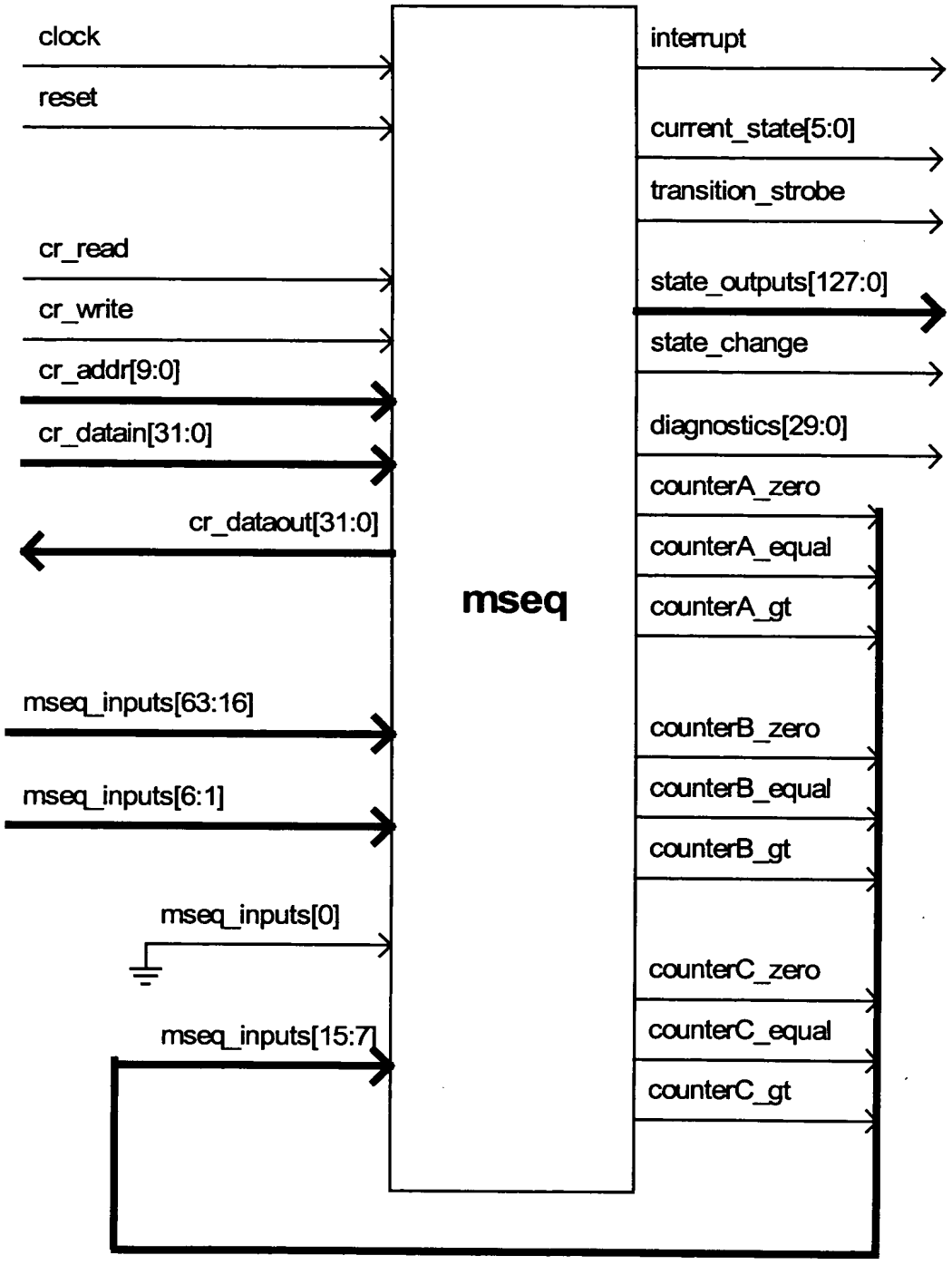

clock
reset
cr_read
cr_write
cr_addr[9:0]
cr_datain[31:0]
cr_dataout[31:0]
mseq_inputs[63:16]
mseq_inputs[6:1]
mseq_inputs[0]
mseq_inputs[15:7]
mseq
interrupt
current_state[5:0]
transition_strobe
state_outputs[127:0]
state_change
diagnostics[29:0]
counterA_zero
counterA_equal
counterA_gt
counterB_zero
counterB_equal
counterB_gt
counterC_zero
counterC_equal
counterC_gt

FIG. 15

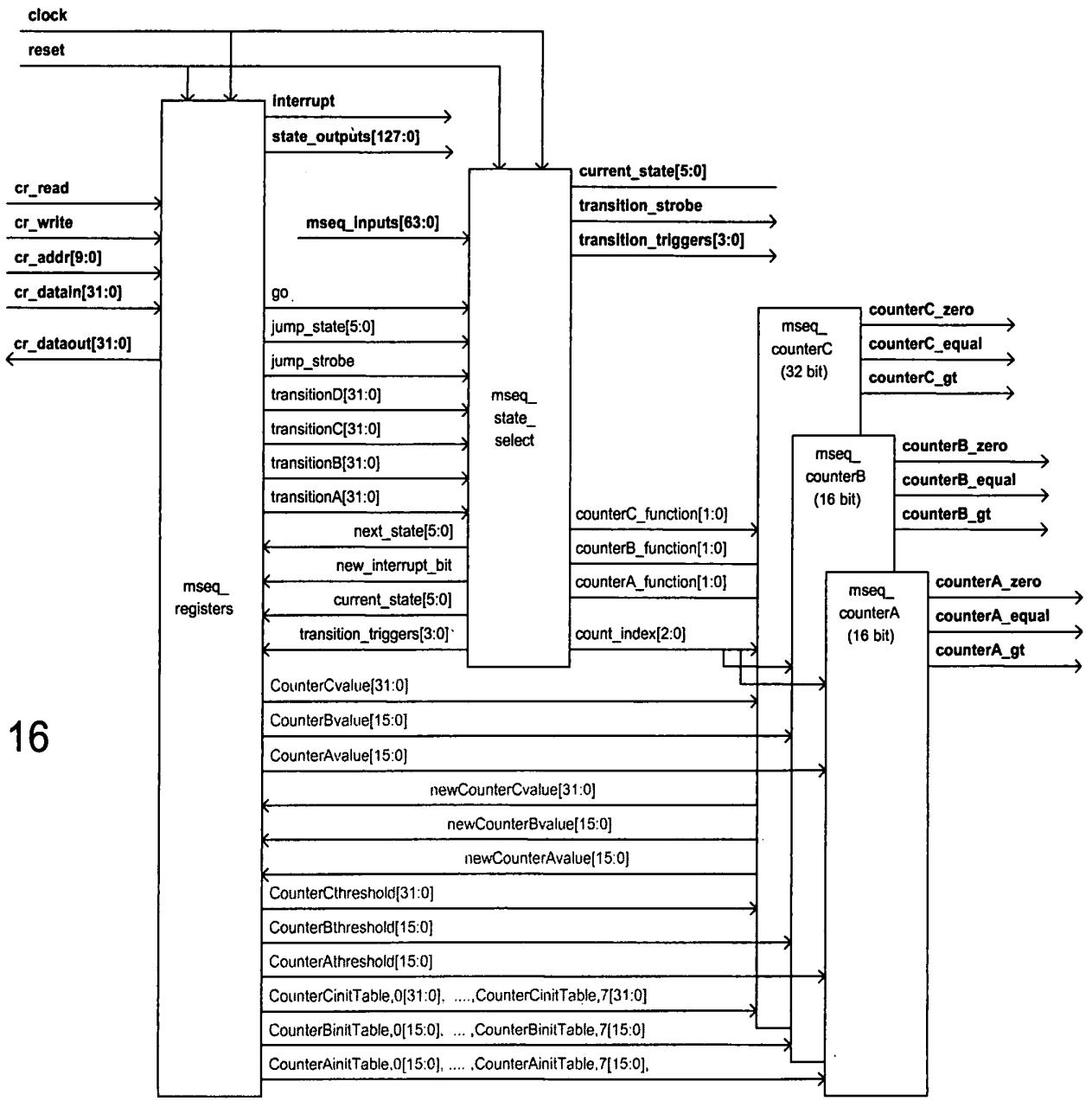
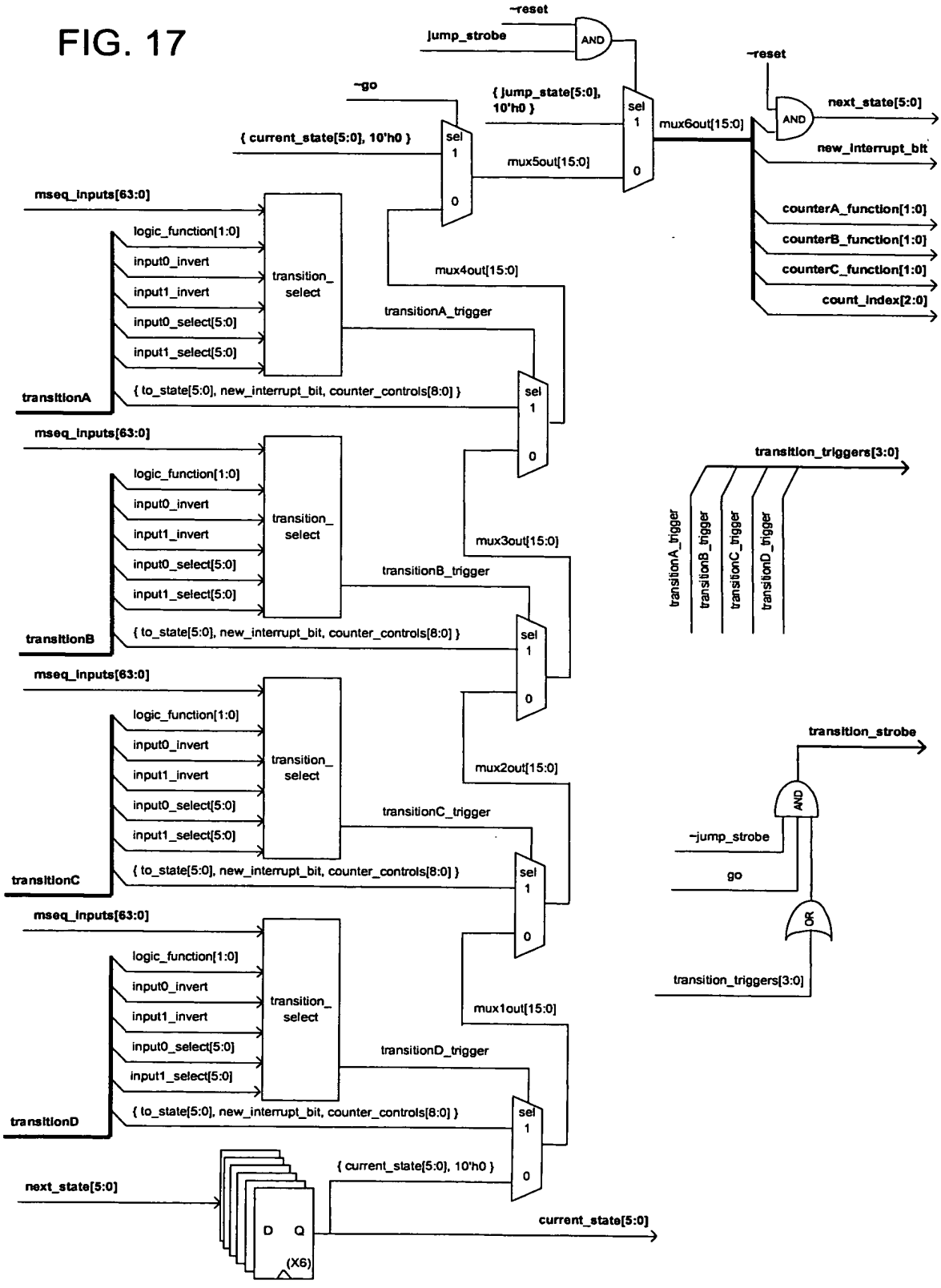

clock
reset
interrupt
state_outputs[127:0]
current_state[5:0]
transition_strobe
transition_triggers[3:0]
cr_read
cr_write
cr_addr[9:0]
cr_datain[31:0]
cr_dataout[31:0]
mseq_inputs[63:0]
go
jump_state[5:0]
jump_strobe
transitionD[31:0]
transitionC[31:0]
transitionB[31:0]
transitionA[31:0]
next_state[5:0]
new_interrupt_bit
current_state[5:0]
transition_triggers[3:0]
mseq_
registers
mseq_
state_
select
counterC_function[1:0]
counterB_function[1:0]
counterA_function[1:0]
count_index[2:0]
mseq_
counterC
(32 bit)
counterC_zero
counterC_equal
counterC_gt
mseq_
counterB
(16 bit)
counterB_zero
counterB_equal
counterB_gt
mseq_
counterA
(16 bit)
counterA_zero
counterA_equal
counterA_gt
CounterCvalue[31:0]
CounterBvalue[15:0]
CounterAvalue[15:0]
newCounterCvalue[31:0]
newCounterBvalue[15:0]
newCounterAvalue[15:0]
CounterCthreshold[31:0]
CounterBthreshold[15:0]
CounterAthreshold[15:0]
CounterCinitTable,0[31:0], ...,CounterCinitTable,7[31:0]
CounterBinitTable,0[15:0], ... ,CounterBinitTable,7[15:0]
CounterAinitTable,0[15:0], ... ,CounterAinitTable,7[15:0],

FIG. 16

FIG. 17


~reset
jump_strobe
AND
~reset
~go
{ jump_state[5:0], 10'h0 }
sel
1
0
mux6out[15:0]
AND
next_state[5:0]
new_interrupt_bit
{ current_state[5:0], 10'h0 }
mux5out[15:0]
counterA_function[1:0]
counterB_function[1:0]
counterC_function[1:0]
count_index[2:0]
mseq_inputs[63:0]
logic_function[1:0]
input0_invert
input1_invert
input0_select[5:0]
input1_select[5:0]
transition_ select
mux4out[15:0]
transitionA_trigger
transitionA
{ to_state[5:0], new_interrupt_bit, counter_controls[8:0] }
transition_triggers[3:0]
transitionA_trigger
transitionB_trigger
transitionC_trigger
transitionD_trigger
mux3out[15:0]
transitionB_trigger
transitionB
mux2out[15:0]
transitionC_trigger
transitionC
transition_strobe
AND
~jump_strobe
go
OR
transition_triggers[3:0]
mux1out[15:0]
transitionD_trigger
transitionD
{ current_state[5:0], 10'h0 }
next_state[5:0]
D
Q
(X6)
current_state[5:0]

transition select diagram

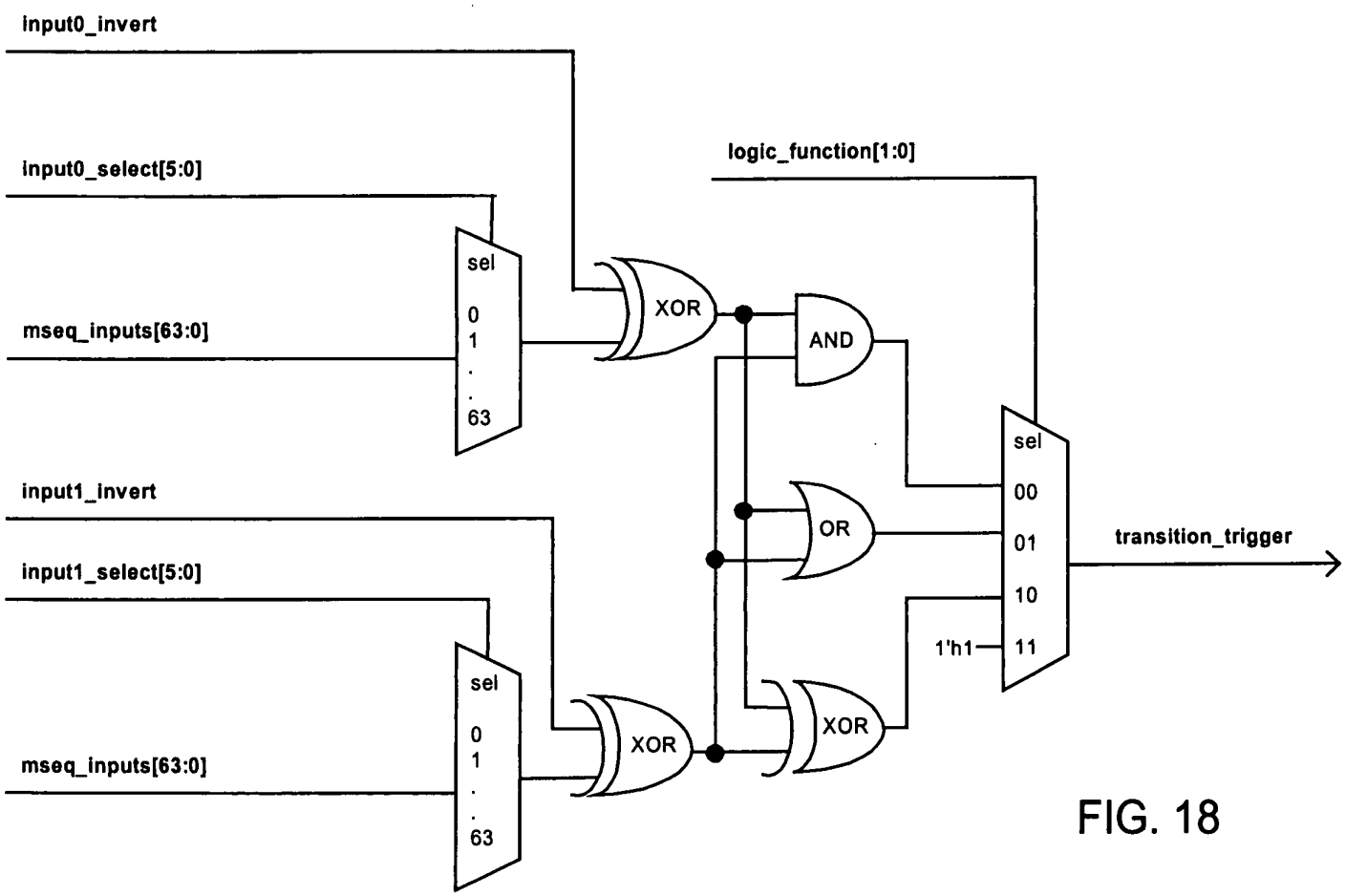


FIG. 18

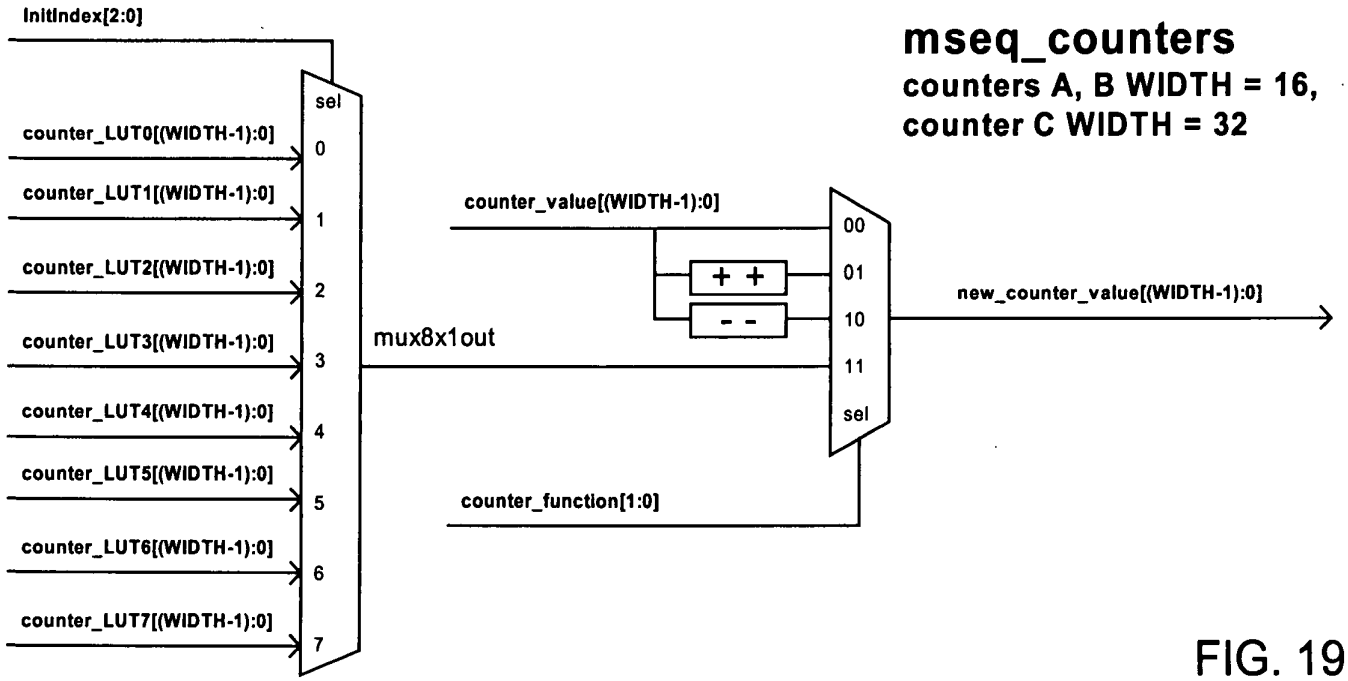
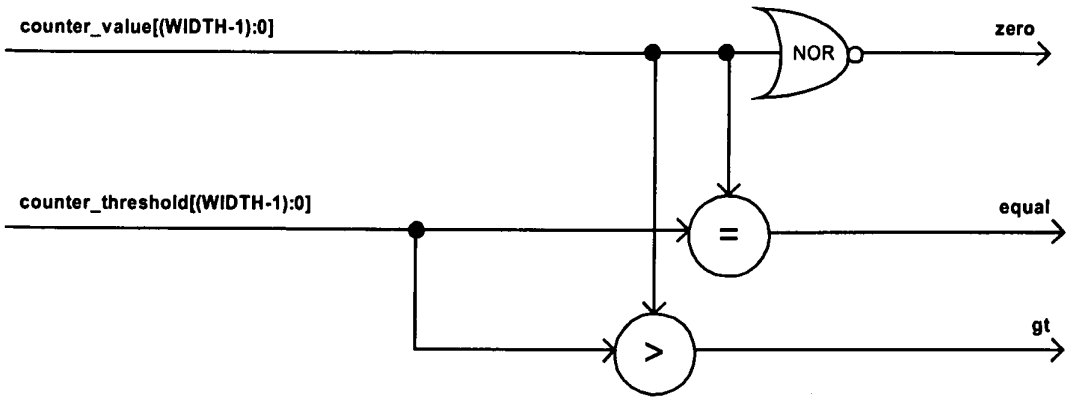

InitIndex[2:0]
sel
counter_LUT0[(WIDTH-1):0]
0
counter_LUT1[(WIDTH-1):0]
1
counter_LUT2[(WIDTH-1):0]
2
counter_LUT3[(WIDTH-1):0]
3
counter_LUT4[(WIDTH-1):0]
4
counter_LUT5[(WIDTH-1):0]
5
counter_LUT6[(WIDTH-1):0]
6
counter_LUT7[(WIDTH-1):0]
7
mux8x1out
counter_value[(WIDTH-1):0]
+ +
- -
00
01
10
11
sel
new_counter_value[(WIDTH-1):0]
counter_function[1:0]
mseq_counters
counters A, B WIDTH = 16,
counter C WIDTH = 32

FIG. 19


counter_value[(WIDTH-1):0]
NOR
zero
counter_threshold[(WIDTH-1):0]
=
equal
>
gt

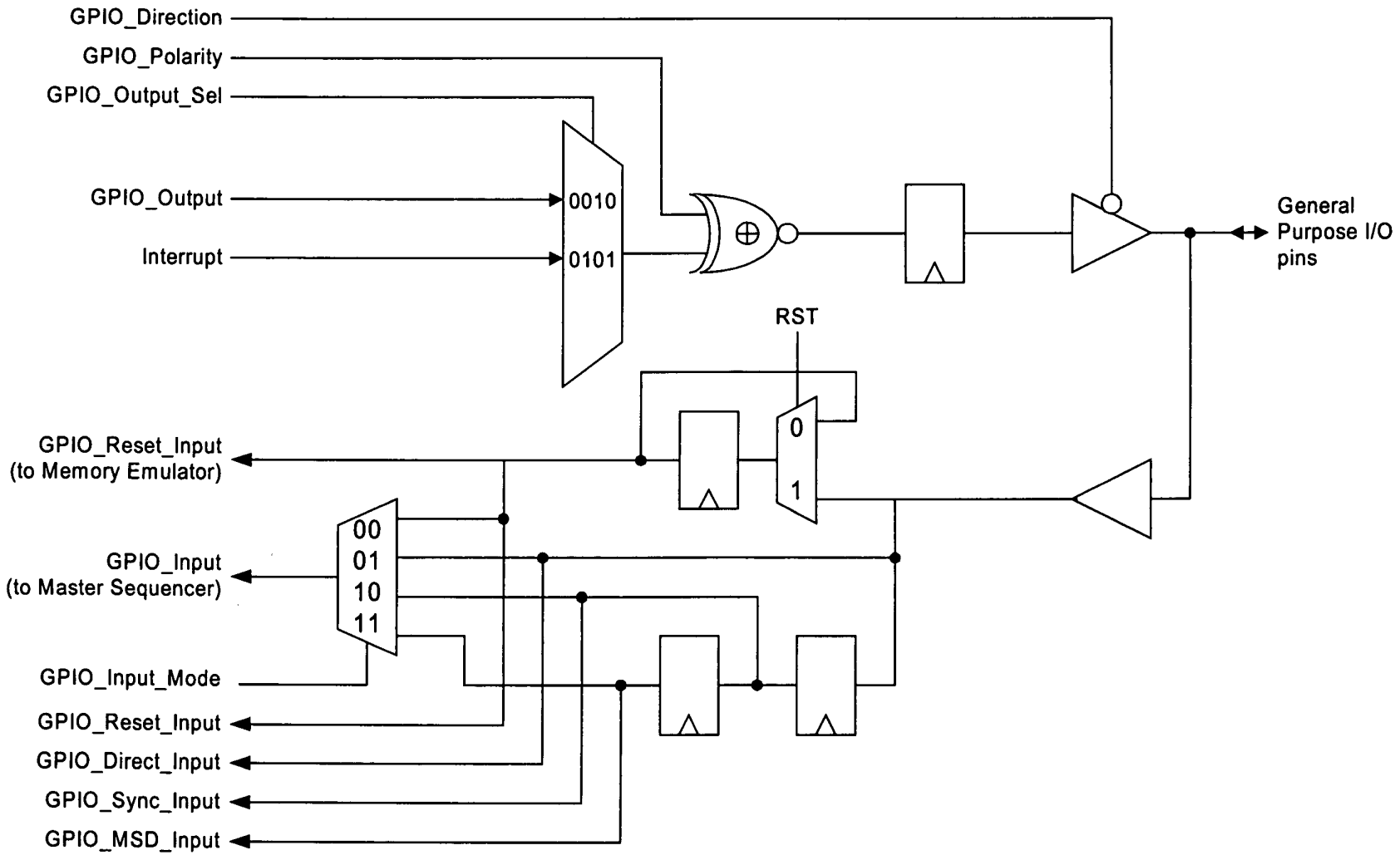

GPIO_Direction
GPIO_Polarity
GPIO_Output_Sel
GPIO_Output
Interrupt
0010
0101
General Purpose I/O pins
RST
0
1
GPIO_Reset_Input (to Memory Emulator)
00
01
10
11
GPIO_Input (to Master Sequencer)
GPIO_Input_Mode
GPIO_Reset_Input
GPIO_Direct_Input
GPIO_Sync_Input
GPIO_MSD_Input

FIG. 20

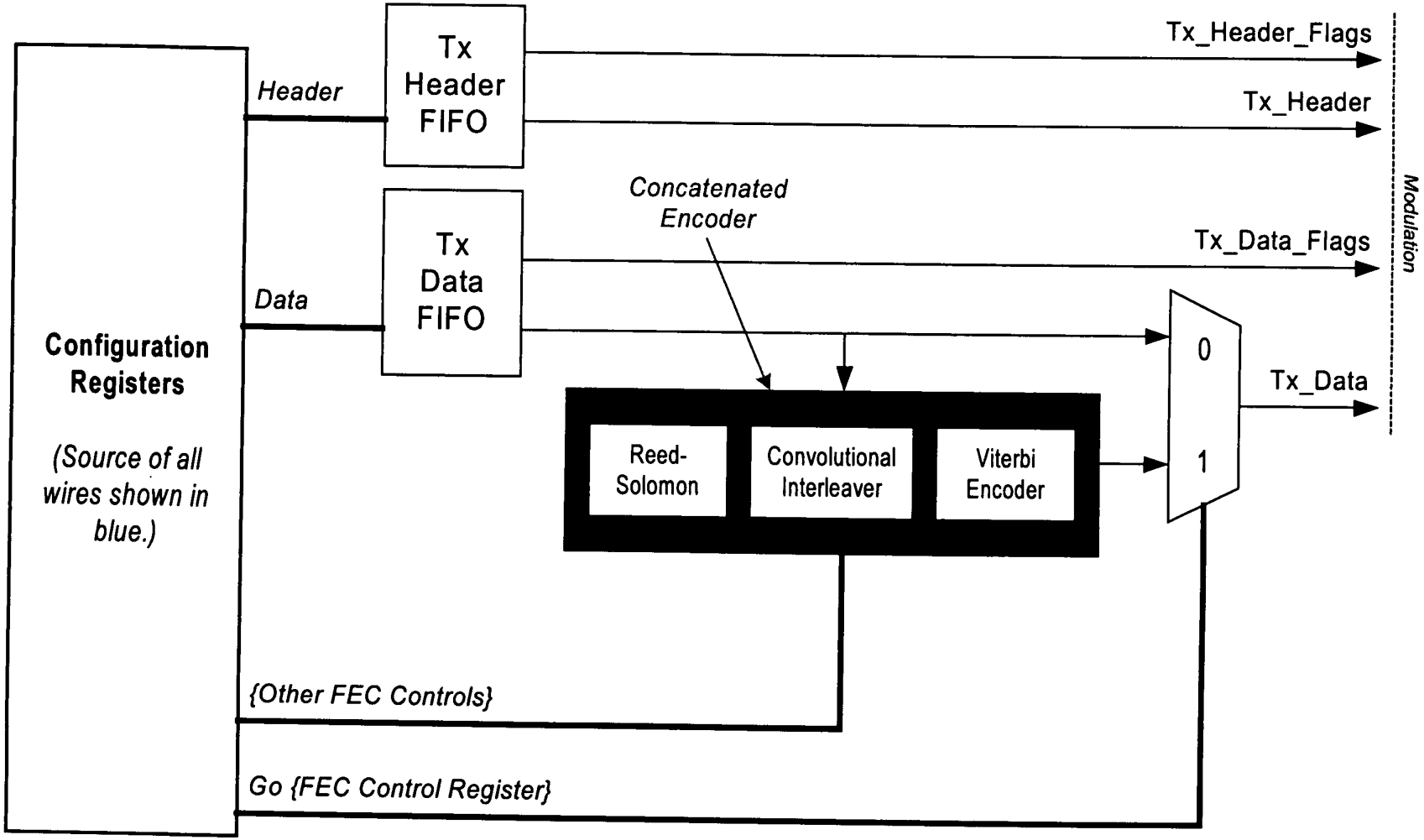
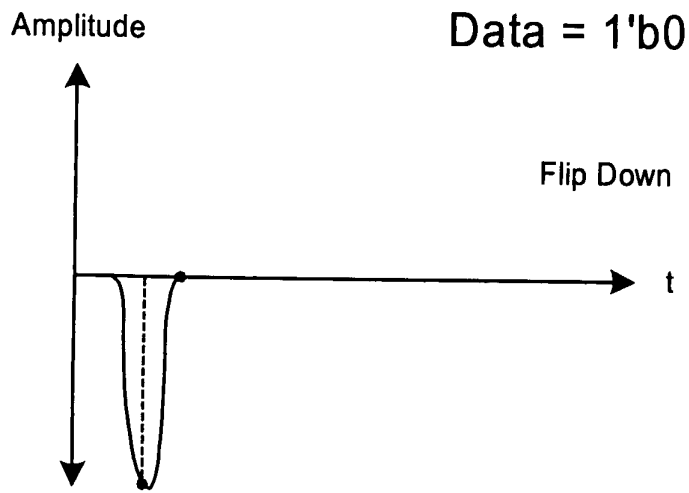

Tx
Header
FIFO
Header
Tx_Header_Flags
Tx_Header
Concatenated
Encoder
Tx
Data
FIFO
Data
Tx_Data_Flags
Modulation
Configuration
Registers
(Source of all
wires shown in
blue.)
0
1
Tx_Data
Reed-
Solomon
Convolutional
Interleaver
Viterbi
Encoder
{Other FEC Controls}
Go {FEC Control Register}

FIG. 21



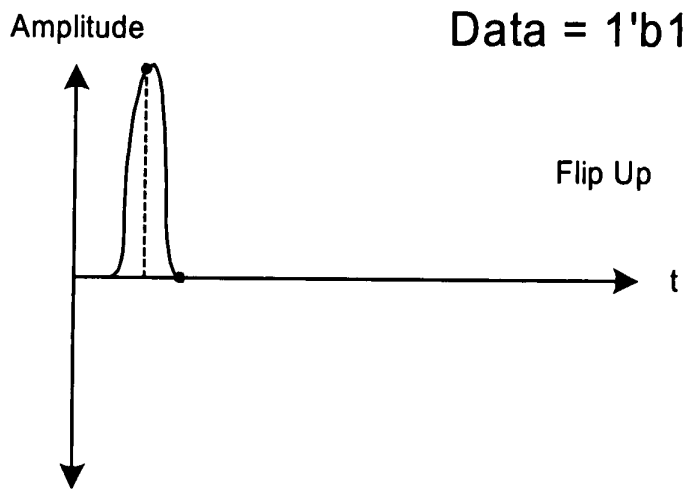
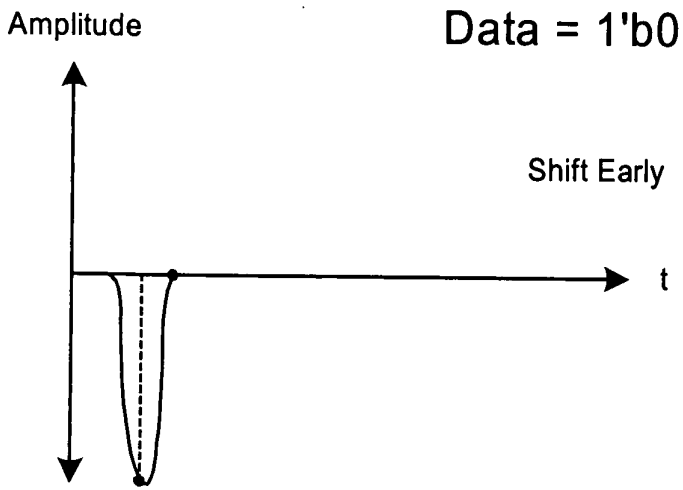


FIG. 22


Amplitude
Data = 1'b0
Shift Early
t

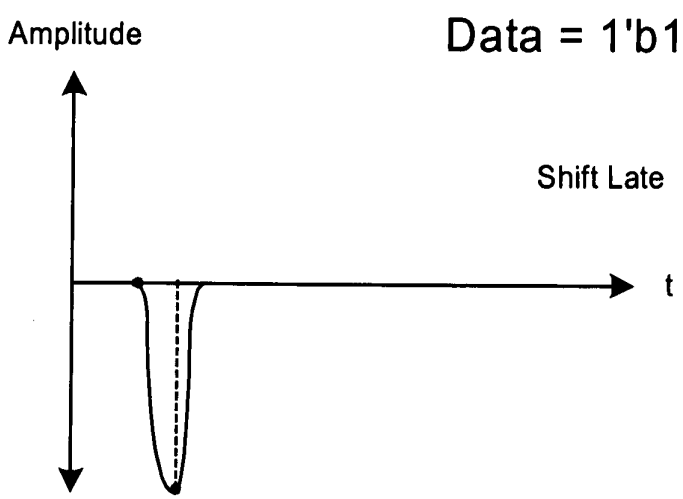

Amplitude
Data = 1'b1
Shift Late
t

FIG. 23

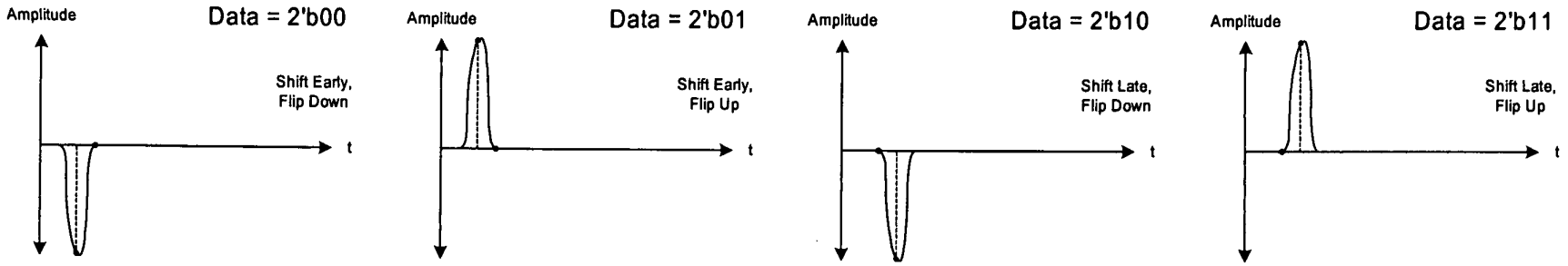

Amplitude
Data = 2'b00
Shift Early,
Flip Down
t
Amplitude
Data = 2'b01
Shift Early,
Flip Up
t
Amplitude
Data = 2'b10
Shift Late,
Flip Down
t
Amplitude
Data = 2'b11
Shift Late,
Flip Up
t

FIG. 24

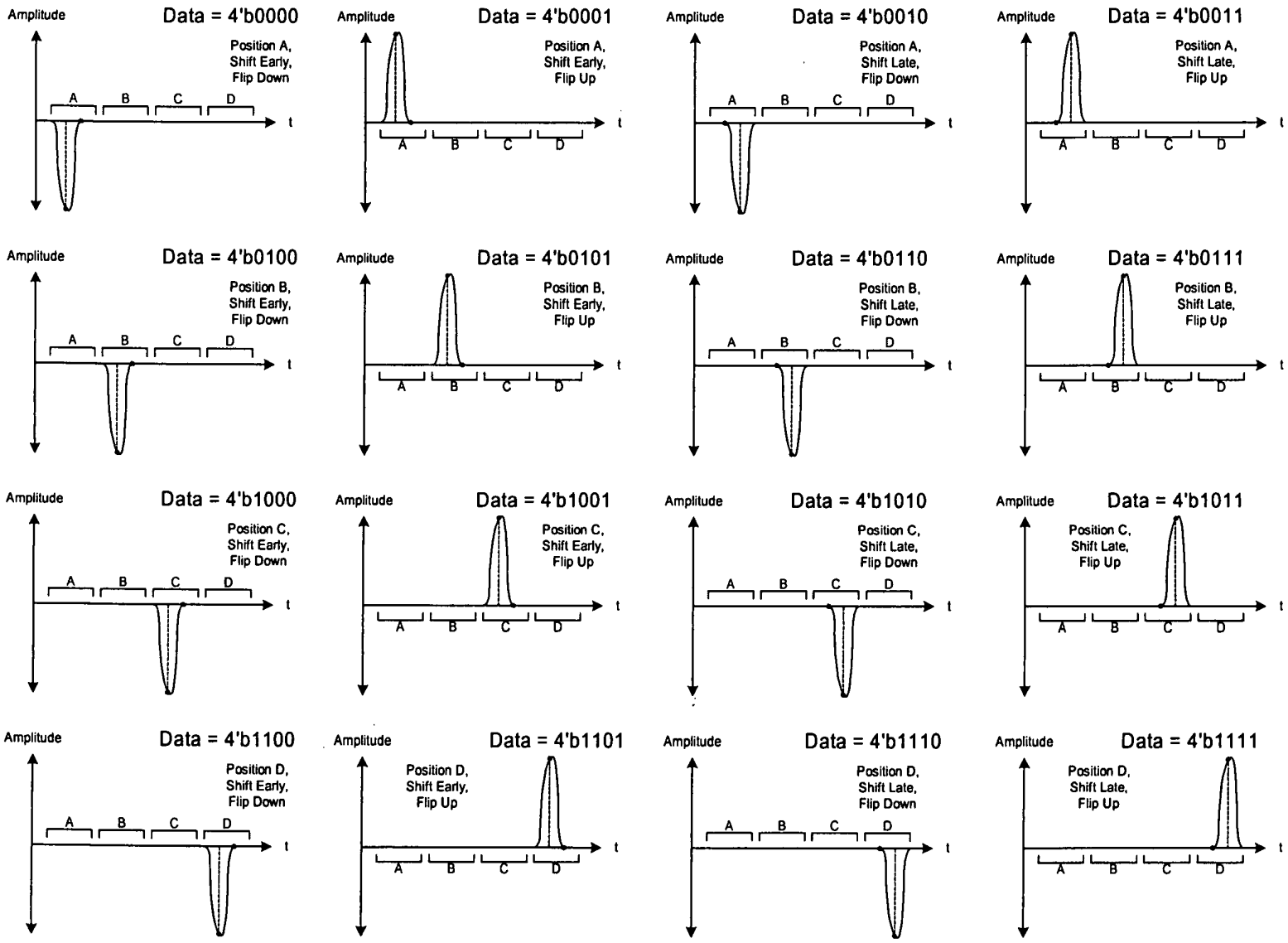

Amplitude
Data = 4'b0000
Position A, Shift Early, Flip Down
Data = 4'b0001
Position A, Shift Early, Flip Up
Data = 4'b0010
Position A, Shift Late, Flip Down
Data = 4'b0011
Position A, Shift Late, Flip Up
Data = 4'b0100
Position B, Shift Early, Flip Down
Data = 4'b0101
Position B, Shift Early, Flip Up
Data = 4'b0110
Position B, Shift Late, Flip Down
Data = 4'b0111
Position B, Shift Late, Flip Up
Data = 4'b1000
Position C, Shift Early, Flip Down
Data = 4'b1001
Position C, Shift Early, Flip Up
Data = 4'b1010
Position C, Shift Late, Flip Down
Data = 4'b1011
Position C, Shift Late, Flip Up
Data = 4'b1100
Position D, Shift Early, Flip Down
Data = 4'b1101
Position D, Shift Early, Flip Up
Data = 4'b1110
Position D, Shift Late, Flip Down
Data = 4'b1111
Position D, Shift Late, Flip Up
A
B
C
D
t

FIG. 25

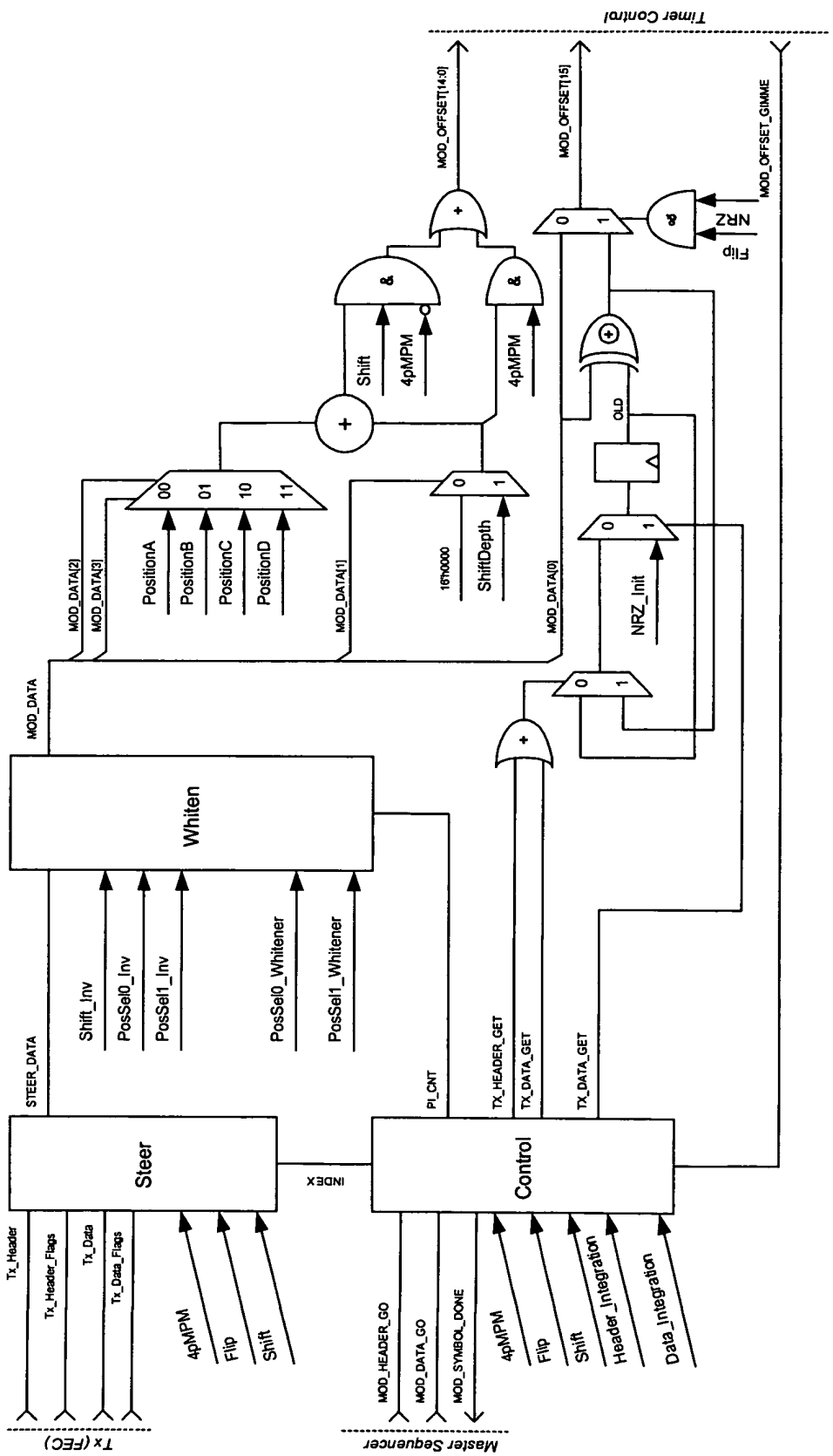

Timer Control
MOD_OFFSET[14:0]
MOD_OFFSET[15]
MOD_OFFSET_GIMME
Flip
NRZ
OLD
NRZ_Init
Shift
4pMPM
4pMPM
PositionA
PositionB
PositionC
PositionD
16'h0000
ShiftDepth
MOD_DATA[2]
MOD_DATA[3]
MOD_DATA[1]
MOD_DATA[0]
MOD_DATA
Whiten
Shift_Inv
PosSel0_Inv
PosSel1_Inv
PosSel0_Whitener
PosSel1_Whitener
STEER_DATA
PI_CNT
TX_HEADER_GET
TX_DATA_GET
TX_DATA_GET
Steer
INDEX
Control
Tx_Header
Tx_Header_Flags
Tx_Data
Tx_Data_Flags
4pMPM
Flip
Shift
MOD_HEADER_GO
MOD_DATA_GO
MOD_SYMBOL_DONE
4pMPM
Flip
Shift
Header_Integration
Data_Integration
Tx (FEC)
Master Sequencer

FIG. 26

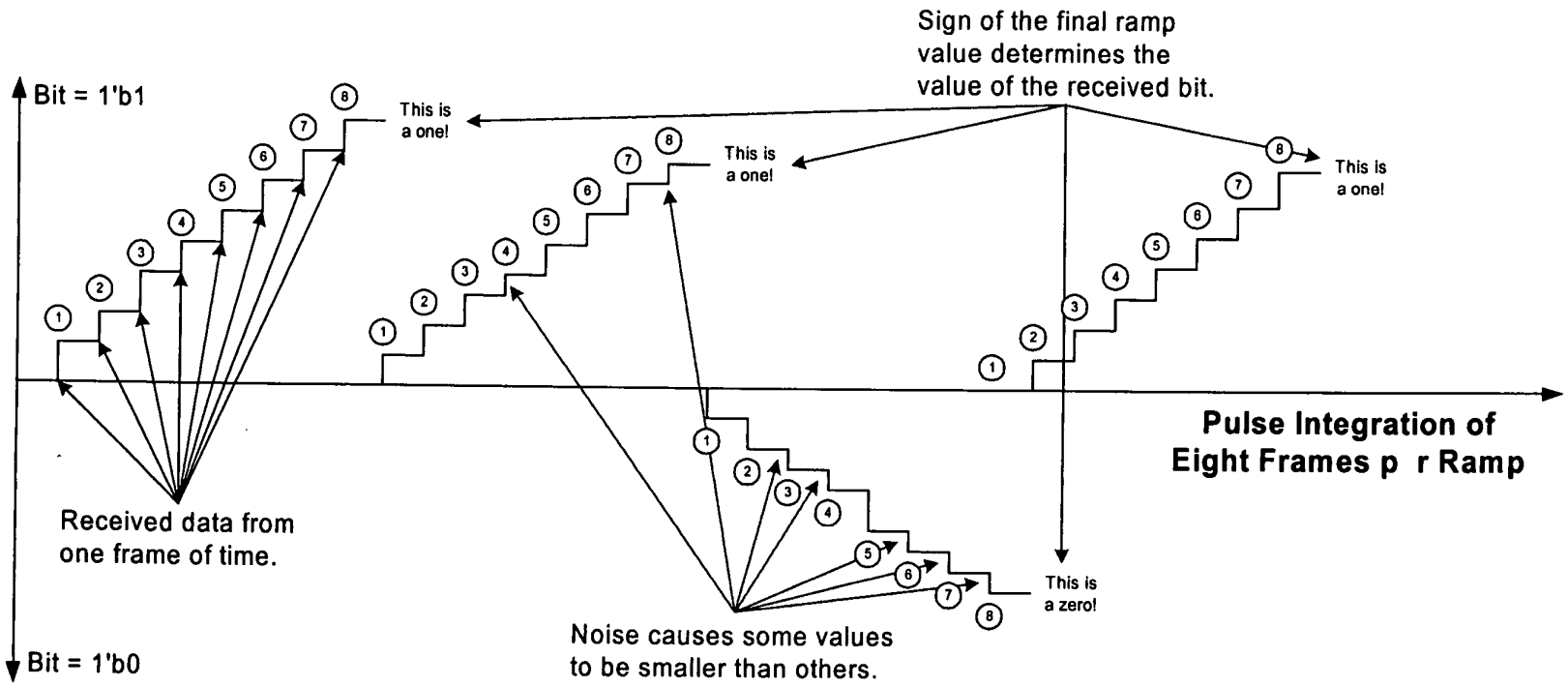

Sign of the final ramp value determines the value of the received bit.
Bit = 1'b1
This is a one!
This is a one!
This is a one!
Pulse Integration of Eight Frames p r Ramp
Received data from one frame of time.
This is a zero!
Noise causes some values to be smaller than others.
Bit = 1'b0

FIG. 27